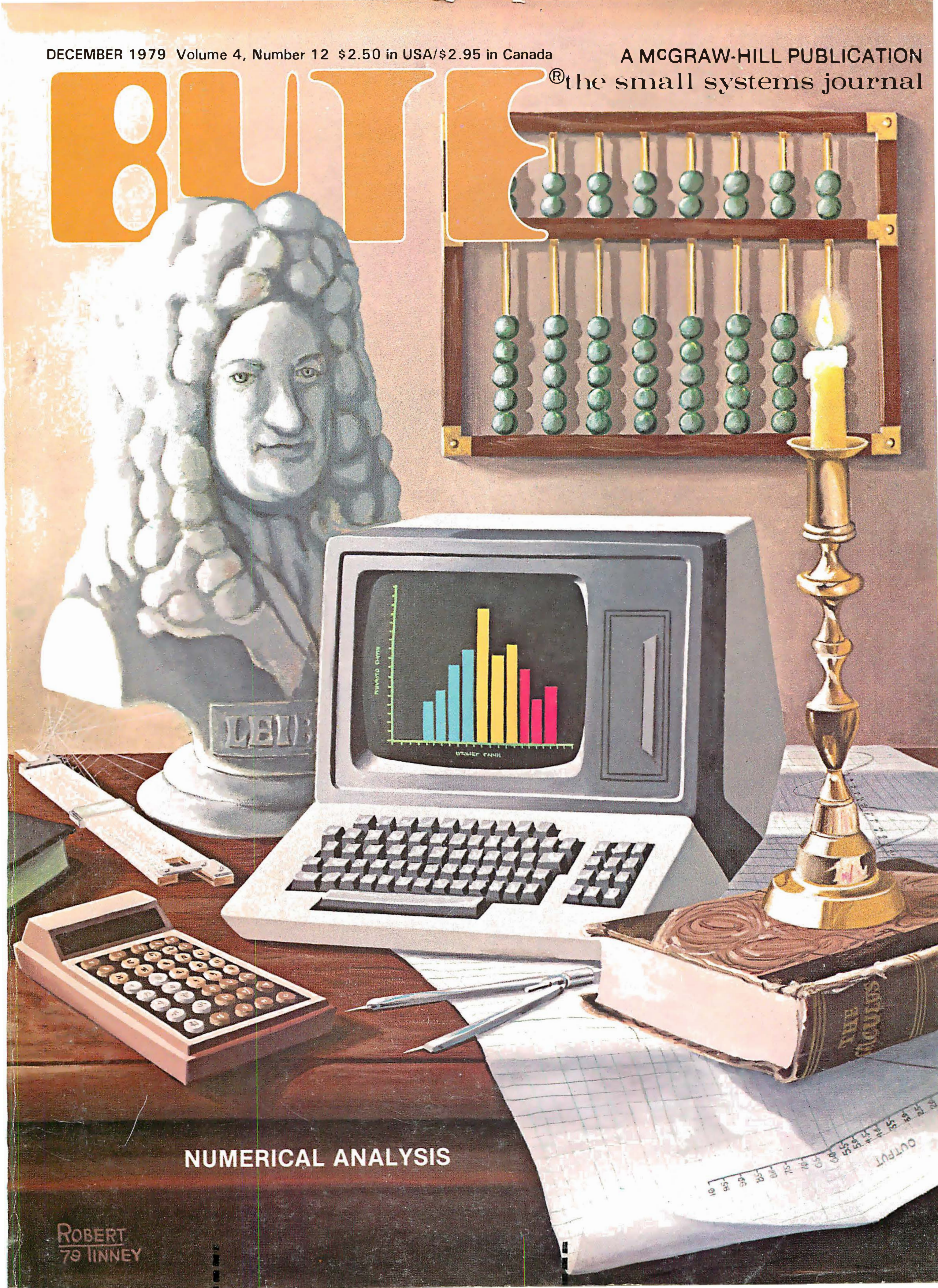


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BYTE
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NUMERICAL ANALYSIS
ROBERT '79 TINNEY



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And the computer has a full 12-slot card cage you can use for additional RAM and interface cards.

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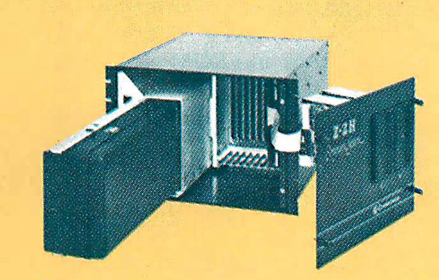
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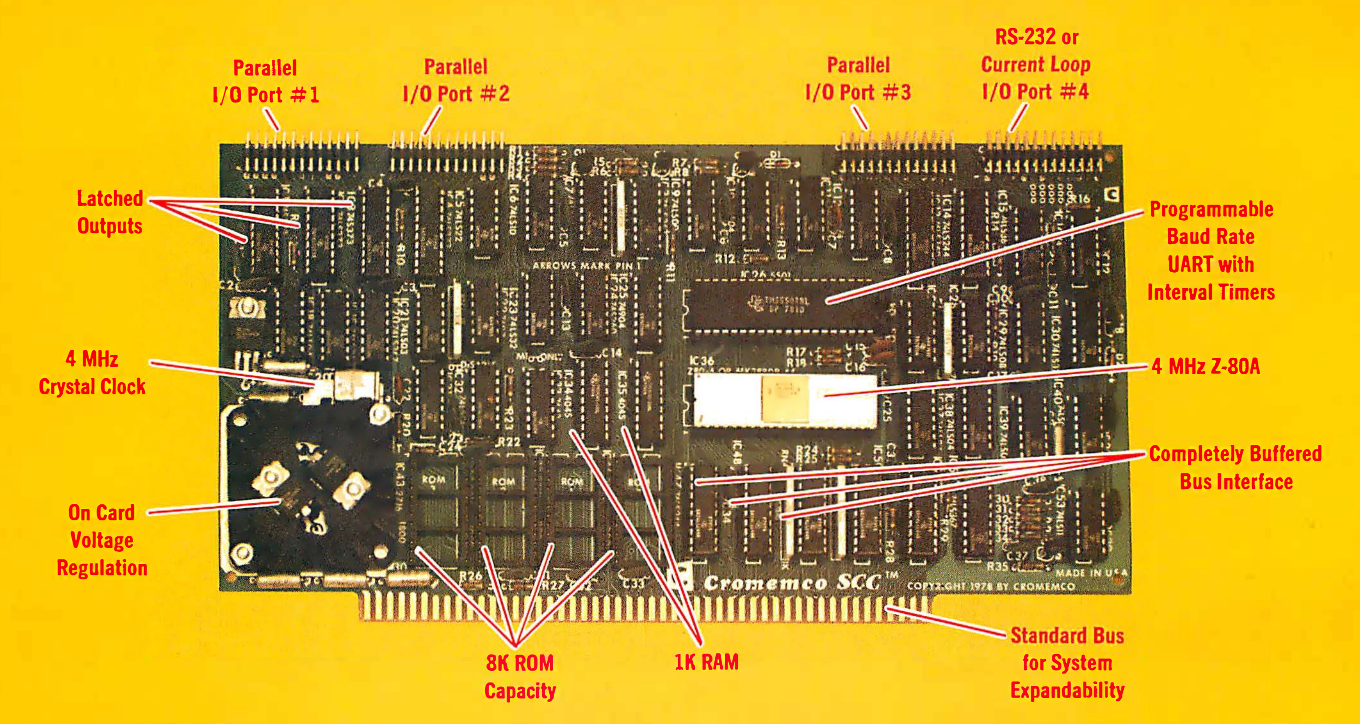
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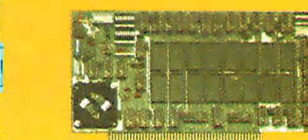
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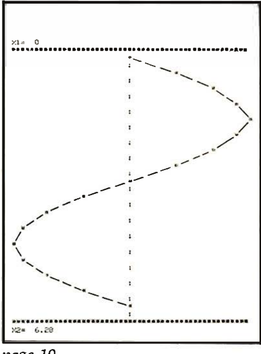
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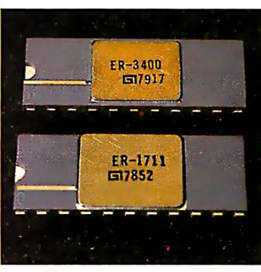
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Nucleus



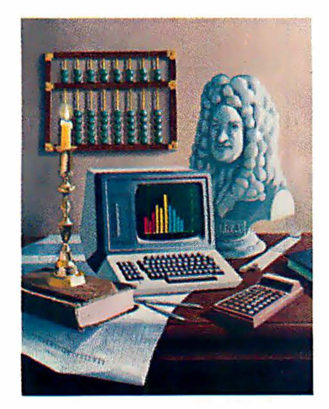
Cover Art: **Numerical Analysis** *by Robert Tinney*

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In This BYTE



About the Cover

This month's cover features artist Robert Tinney's concrete realization of the theme for several articles in this issue: today's tools of analysis and design are computers, both as calculating-engines and as non-traditional symbol-manipulators. By implication, if Leibniz were alive today he would be employing a friendly desk-top computer as a tool for examination of concepts ranging far beyond the calculus he helped shape.

The Fast Fourier Transform (FFT) is a unique algorithm that is necessary for the analysis and reproduction of signal waveforms. However, performing a complex mathematical derivation of the concept is not necessary. Fred Ruckdeschel has formulated a nonrigorous mathematical treatment of the FFT and demonstrates how it may be applied to synthesize a variety of waveforms in the **Frequency Analysis of Data Using a Microcomputer.**

Page 10

Does data evaporate from your computer's volatile programmable memory when you turn the power off? Perhaps you could benefit from having some nonvolatile memory in your machine. Steve Ciarcia explores the useful properties of electrically alterable read-only memory as he tells how to **Add Nonvolatile Memory to Your Computer.**

Page 36

After finding software-intensive approaches to audio processing too slow for high fidelity sound, William J Dally set out to develop a system that uses hardware to speed up processing of audio signals. He explains his ideas in **Faster Audio Processing with a Microprocessor.**

Page 54

Huffman code is a method for compressing text characters by exploiting their relative frequency of occurrence in text. Space savings of up to 50% can be realized using this technique. James Peterson discusses the advantages and tradeoffs involved in this and other types of **Text Compression.**

Page 106

Numerical analysis techniques are quite often simplified by the use of powerful number handling algorithms available on large computer systems. A reasonable alternative to such analysis for the small-scale computer user lies in the utilization of the hand calculator. Small calculators continue to expand their capabilities as proven by Pierre Chance in his investigation of **Analysis of Polynomial Functions with the TI-59 Calculator.**

Page 120

Most methods of estimating a particular function and plotting it require an analysis involving calculus. Timothy Bowker has written a program that performs a simple trigonometric analysis of a function which will yield an accurate approximation of the function and then print the curve on a Hewlett-Packard 9872A plotter. See his article entitled **Minimizing Curve-Plotting Calculation.**

Page 134

In the analysis of system response, the utility of the transfer function is immeasurable. The transfer function will convert a time domain relationship into a frequency domain relationship, a manipulation that can prove to simplify the solution process. Bryan Finlay presents a clear picture of the concepts involved in a **Noniterative Digital Solution of Linear Transfer Functions.**

Page 144

The usefulness of microcomputers is increasing as more powerful and varied programming languages are implemented. Christopher Kern provides **A User's Look at Tiny-c,** one of the more recent languages to appear.

Page 196

Some Notes on Modular Assembly Programming presents several examples of well-written assembler programs. James Lewis feels that a structured approach to program writing helps both the design and implementation processes.

Page 222

Many people use loops in computer programs without really thinking about how they work. In **Twenty-four Ways to Write a Loop,** W D Maurer illustrates the endless variety of program loops and shows you how to get the most out of them.

Page 241

If you're interested in using your computer to learn Morse code, Mark Bernstein's **Morse Code Trainer** can help you to practice. His program translates plain text into Morse code and then outputs it through a speaker.

Page 247

Does it take you ten minutes to enter twenty lines of code at your terminal? Are your index fingers worn out from hours of hunting and pecking? Why not use your own computer to learn the useful art of touch typing. Read Arthur Armstrong's article, **Thirty Days To a Faster Input.**

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Editorial

On the Importance of Casting Abstractions in Concrete

Carl Helmers

We human beings are a conceptual species. While firmly planted in our animal evolutionary roots, our chief distinguishing characteristic is a degree of development of our mental powers. This characteristic allows us to recursively reflect upon the degree of development of our mental powers,among other things. The idea of a computer as a mental amplifier fits well within this conceptual side of human nature. In part, this explains the intellectual fascination of computing technology, which is available on a widespread basis as the modern personal computer. As a thought recording and amplification device, the computer deals with abstractions admirably. But there is also another side to the human fascination with computing which should not be ignored: the casting of abstractions in concrete forms which are understandable and emotionally gratifying. Here we find the animal side of our evolutionary heritage interacting with the cerebral side, producing a positive human value for an otherwise sterile activity.

Conceptualization exists in human beings. We do it all the time, for it is a part of our nature. Some do it better than others. Like any ability, it varies from individual to individual. Within individuals this ability varies over the course of a lifetime of growth, development and aging.

The content of our thoughts can be explicit models closely bound to the real world as perceived by human senses, abstractions like those of mathematics which are less obviously bound to real-world roots, or even total fantasies such as stories of science fiction, novels, plays, paintings and other forms of art. *All* innovation and progress start out as a conceptual fantasy, whether or not the fantasy is based on real-world inputs. But, if the fantasy is to be imparted to someone or made into a real-world object, it must be figuratively "cast in concrete" as a tangible and specific item. I make the claim that one tie with our evolutionary past is partly demonstrated by the emotional experience of pleasure derived by seeing concrete and specific results come from efforts directed by an abstract plan.

This is the phenomenon of emotional feedback from intellectual activites, made "real" in some way as a specific action. As I write these words at a keyboard, I am illustrating the phenomenon in the pleasure I derive from formulating my words into an essay. The concepts are certainly in my own mind. I am translating them through specific actions into a concrete form: the words printed on a piece of paper in the form of a draft I send to our copy editors.

In an analogous way, a writer of a science fiction story is a spinner of tales. Such tales are but dreams bottled up in a mind unless they are cast into a concrete form signifying meaning: as an oral or written account transmitted to another mind. We only know that the science fiction spinner of tales exists at all because of this concrete form of his or her fantasy abstractions.

For the fascination of computing, there is ample opportunity for casting abstract concepts into concrete form. Here we get the emotional feedback and confirmation of our understanding about the way a system of concepts works in a specific example. The importance of game programming on computers as a way of learning to write programs and learn about interactive sequences cannot be underestimated.

"My Shugart followed me home."

"After working all day with the computer at work, it's a kick to get down to Basic at home. And one thing that makes it more fun is my Shugart minifloppy™. We use Shugart drives at work, so when I bought my own system I made sure it had a minifloppy drive.

"Why? Shugart invented the minifloppy. The guys who designed our system at work tell me that Shugart is the leader in floppy design and has more drives in use than any other manufacturer. If Shugart drives are reliable enough for hard-working business computers, they've got to be a good value for my home system.

"When I'm working on my programs late at night, I can't wait for cassette storage. My minifloppy gives me fast random access and data transfer. The little minidiskettes™ store plenty of data and file easily too.

"I made the right decision when I bought a system with the minifloppy. When you lay out your own hard-earned cash, you want reliability and performance. Do what I did. Get a system with the minifloppy."

If it isn't Shugart, it isn't minifloppy.



435 Oakmead Parkway, Sunnyvale, California 94086

See opposite page for list of manufacturers featuring Shugart's minifloppy in their systems.

The act of defining a game as a program and making a specific implementation is this very act of casting an abstraction (the game) into concrete form (the program which allows one to interact with that abstraction).

Just as I cannot partake of the science fiction writer's tale without a concrete form of sensible representation, I cannot play some adventure game in someone else's head. I can play the game only in the concrete form of its traditional letter correspondence mode (a la Dungeons and Dragons) or the computer automated forms of a specific program (with names like Adventure, Zork, etc). This abstraction which is the concept of the game cannot be perceived emotionally except in this form of a specific implementation.

The pleasure of seeing an abstract concept transformed into a concrete representation is one of the key motivations of the experimenter. The experimenter is the person who works creatively with a technology — be it oil paints on canvas or bit patterns in memory — and sees the results at first hand. It is the spirit of the scientist as much as of the artist.

Why should I sit down and design a computer, then build it, then design my own particular style of system software? There are numerous wheels in the computer world which at first sight I do not need to reinvent in various ways. But the way to thoroughly understand an art, science or technology is to participate in it. Thus, I spend effort designing and building computer systems from time to time; I spend effort now and then designing and implementing text editors; I spend effort from time to time designing and implementing simple interactive application programs for mundane tasks. I do not do this without a return on my efforts in the form of the emotional satisfaction and pleasure which come from seeing my abstract concepts implemented in concrete form.

I partake of the pleasure of exploring the possible concepts of a design, settling on one, then working out its hidden implications and feeding that knowledge back into the design. This is the challenge of understanding which motivates our curiosity in any field. It is made quite explicit by the demands of the computer field. Programming a computer is a very abstract concept, yet when that computer program abstraction turns on a motor in a robot arm, or sounds a note on a music synthesizer in a progression of some fugue, the program has a very real and concrete way of interacting with our senses and emotional evaluations.

This, then, is the true importance of experimentation and the resultant casting of abstract ideas into concrete form: it provides us with emotional confirmation via pleasure of an otherwise valueless thought. The human value of pleasure, or happiness, in turn feeds back into our thought processes, and the cycle continues. The act of translation, from abstract to concrete, aids us in our understanding of the world and our perceptions of it. ■

Progress Report: The 6809 Project

At this writing, September 26 1979, my 6809's central processor card design is complete in the form of a wiring diagram spread over four large sheets of drafting vellum. I have not yet begun to wire the processor, due to a heavy travel and speaking schedule in late summer and early autumn of this year. Once I have finished the actual implementation of the card, readers can expect to see photographs, wiring diagram, and hand-assembled machine language primitives for a terminal-oriented operating system. Timing? As noted earlier, I continue with this project at the sufferance of a 24-hour day. So, the next installment will come when it is ready, and no sooner. ...CH

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Frequency Analysis of Data Using a Microcomputer

F R Ruckdeshel
773 John Glen Blvd
Webster NY 14580

Introduction

People involved with digital electronics often deal with signals in which the voltage or current changes with time. When a pulse is distorted, its shape is generally expressed in terms of *overshoot* or *rise time*.

In the design of analog electronics equipment such as audio amplifiers, great emphasis is placed on frequency response and phase shifts. The performance of consumer-oriented audio systems is not normally specified in terms of pulse rise time or pulse delay. However, such a specification would characterize the system's basic response to the *zeroth order*. The zeroth order qualifier is necessary because rise time is only an approximate (but very useful) description of a system's response to a stepped input. A complete description would be possible through comparative plots of input and output waveforms.

In communications theory both the real-time (signal versus time) and frequency (signal content versus frequency) representations are applied somewhat interchangeably since the object is to transmit real-time signals, such as pulses, over channels having bandwidth and noise limitations. The Fourier transform is used to aid in such analyses. To exercise this analysis technique it is assumed that the system response is linear. That is, if the input signal level is halved, so is the output signal, along with no change in signal shape. It is thus apparent why most digital engineers do not use Fourier transforms; their systems are highly nonlinear, and work well because of the nonlinearity. It is also apparent why audio engineers are heavily dependent on frequency analysis; their systems are highly linear.

The choice of the Fourier transform for electronics analysis is based on the properties of its "basis" functions, sinusoids. For example, in electronic systems which are composed of ideal inductors, resistors and capacitors, sinusoids have the unique property that if a pure sinusoid of a particular frequency is inserted anywhere into a circuit, examination of any other location in the circuit will show a pure sinusoid of the same frequency, though perhaps changed in amplitude and phase. There is no *mode conversion*. In real systems, however, nonlinearities in response can lead to *harmonic distortion*, which is another way of saying *mode conversion*.

Vital to the application of sinusoids in Fourier analysis is a property called *linear independence*. That is, it is not possible to generate a sinusoid of angular frequency w_1, from the addition (a linear operation) of two other sinusoids having frequencies w_2 and w_3 ($w_1 \neq w_2, w_3$). A nonlinear operation such as multiplication is required for this to occur.

Mathematically speaking, the sinusoidal functions used in Fourier analysis form a complete, continuous, and infinite set of orthogonal functions spanning the space of all real numbers. This should be compared with the analogous digitally-oriented Walsh functions (See "Walsh Functions," September 1977 BYTE, page 190). The Walsh functions form a complete, discrete (but infinite) set of orthogonal functions, also capable of spanning all real space.

Having discussed the basic utility of the functions which compose the Fourier transform, we will now take a brief look at the mathematical structure that will eventually be encoded into a program to calculate frequency transforms.

The Fourier Transform

The basic definition of the Fourier transform operation is:

$$F(w) = \int_{-\infty}^{+\infty} f(x)e^{-iwx}\,dx \qquad (1)$$

where:

$F(w)$ = the frequency transform
$f(x)$ = the function to be transformed
w = the frequency variable (eg: radians/second)
x = the spatial variable (eg: time in seconds)
$i = \sqrt{-1}$

The transform is performed using complex coordinate ($\sqrt{-1}$) algebra and integration. $F(w)$ is thus in the complex domain and is only a mathematical construct. However, $|F(w)|$, the absolute value (or modulus of $F(w)$, is a measurable value. It is defined as:

$$|F(w)|^2 = F^*(w)\ F(w) \quad (2)$$

The * operator stands for conjugation (reversing the signs of the imaginary terms). We note that:

$$F^*(w) = \int_{-\infty}^{+\infty} f(x)^*\ (e^{-iwx})^*\ (dx)^*$$

If x and $f(x)$ are real (as we will now specify), then we have $x^* = x$ and $f(x)^* = f(x)$, giving:

$$F^*(w) = \int_{-\infty}^{+\infty} f(x)\ e^{+iwx}\ dx = F(-w)$$

Thus:

$$F(w) = \sqrt{F(-w)\ F(w)} = F(-w) \quad (3)$$

Note that, in principle, when performing the integration called for in equation (1), all values of w should be considered, both positive and negative. But since equation (3) indicates that $F(w)$ is symmetrical about $w = 0$, we need only consider (and plot) the function for $w \geq 0$.

$|F(w)|$ is called the *amplitude* or *modulus* of the transform. There is also a phase term in the transform which complements the modulus description. For the purposes of this article, however, the phase term will not be considered.

To calculate $|F(w)|$, we observe that:

$$|F(w)|^2 = \{Re\ F(w)\}^2 + \{Im\ F(w)\}^2 \quad (4)$$

The *Re* and *Im* operators denote that the real and imaginary part of $F(w)$ are to be taken respectively. These are:

$$Re\ F(w) = \int_{-\infty}^{+\infty} f(x)\ cos\ (wx)\ dx \quad (5a)$$

$$Im\ F(w) = \int_{-\infty}^{+\infty} f(x)\ sin\ (wx)\ dx \quad (5b)$$

To finally arrange the above equations into a structure suitable for computer calculation, we consider $f_i = f(x_i)$ to represent the data value (perhaps from an equation or experiment) at position x_i. For simplicity we consider the data points to be equally spaced; $x_{i+1} - x_i = \triangle x$.

We also consider f_i to exist only over the interval x_1 to x_N. Outside that interval, f_i will be defined to be zero. Combining the above considerations into a programmable form we have:

$$|F(w_j)|^2 = \{\Sigma_{i=1}^{N} f_i cos\ (w_j x_i) \triangle x\}^2 + \{\Sigma_{i=1}^{N} f_i sin (w_j x_i) \triangle x\}^2 \quad (6)$$

Equation (6) is the basis for the present computer calculation of the Fourier transform of the function represented by $\{f_i\}$. The computer program shown in listing 1 performs this calculation and plots the results.

Note that the number of input data points is N. For an equivalent, but not redundant frequency space description, $N/2$ transform points are required. From an inspection of equation (6) it is apparent that the number of calculations increases by N^2 if a numerical implementation of the integration is applied. Thus, if the number of data points is doubled, the computing time roughly quadruples. The Fast Fourier Transform (FFT) algorithm reduces this dependence. For limited data sets (less than fifty data points), the routine shown in listing 1 takes on the order of fifteen minutes or less in North Star BASIC on an IMSAI, which is acceptable when compared to the large programming complexities associated with implementing an FFT for an arbitrary length data set. The trade-off is between available programmer's time and processor time; my computer lost in the trade-off.

For those interested in further investigation of Fourier transform techniques, an excellent book on the subject is *The Fast Fourier Transform* by E O Brigham, published by Prentice-Hall. Brigham not only presents FFT algorithms, but also reviews continuous transform theory, as well as the errors (particularly at high frequencies) associated with discrete transforms such as the one used here. He also considers reconstruction of the original data set using the calculated frequency transform.

The Discrete Fourier Transform Program

The computer program presented in listing 1 is written in North Star BASIC and is user-oriented. It allows the scale of the automatic data and frequency plots to be adjusted to fit the available terminal width. All plots are shifted and scaled such that they use the maximum terminal width established by the user. Thus, even the owner of a thirty-two-character wide video display can use this program.

The program requires the beginning and ending coordinates (X_1 and X_2 respectively) of the data set as well as

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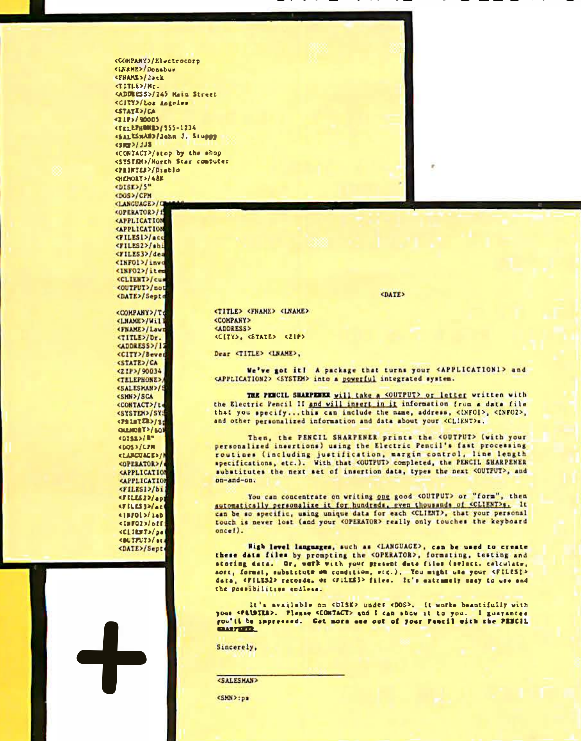
You:

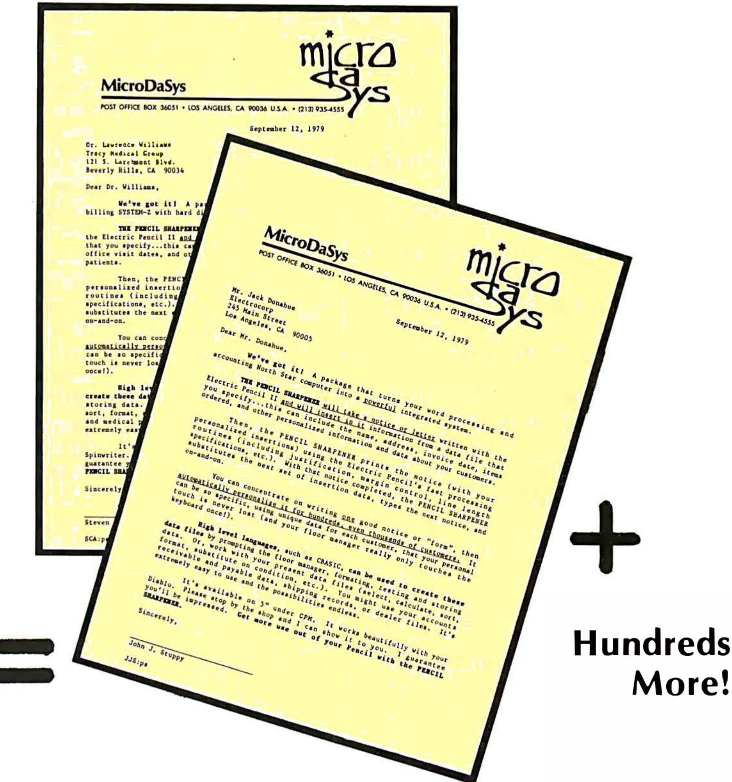
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Listing 1: *This program will input and plot the data set, then determine the transform and display it graphically. The program is written in North Star BASIC, but features particular to this BASIC were avoided so that the software may be run on most BASIC interpreters.*

```
10 REM ***FREQUENCY ANALYZER***
20 REM F. RUCKDESCHEL  9/20/77
30 PRINT\PRINT\PRINT
40 PRINT "***FOURIER SPECTRUM ANALYZER***"
50 PRINT\PRINT
60 PRINT"THIS PROGRAM TRANSFORMS "
70 PRINT"EQUAL INCREMENT DATA INTO "
80 PRINT"FREQUENCY SPACE "
90 PRINT\PRINT
100 PRINT"THE USER INPUTS THE STARTING "
110 PRINT"AND ENDING COORDINATES, ALONG "
120 PRINT"WITH THE NUMBER OF DATA POINTS "
130 PRINT"THE PROGRAM WILL THEN PLOT "
140 PRINT"THE DATA AND ITS SPECTRUM"
150 PRINT\PRINT
160 REM INITIALIZATION
170 PRINT "INPUT TERMINAL WIDTH: ",
180 INPUT L
190 PRINT "BEGINNING CORDINATE: ",
200 INPUT X1
210 PRINT "ENDING COORDINATE: ",
220 INPUT X2
230 PRINT "NUMBER OF DATA POINTS: ",
240 INPUT N
250 PRINT"INPUT SCALE FACTOR: ",
260 INPUT I
270 IF I<1 THEN GOTO 250
280 DIM D(N)
290 D=(X2-X1)/(N-1)
300 W1=0\W2=3.14159/(D*I)
310 W3=W2/(N-1)
320 REM DATA INPUT
330 PRINT "INPUT DATA"
340 FOR I=1 TO N
350 PRINT I,\INPUT D(I)
360 NEXT I
370 B=0
380 REM SHIFT DATA TO NON-NEGATIVE
390 FOR I=1 TO N
400 IF B>D(I) THEN B=D(I)
410 NEXT I
420 FOR I=1 TO N
430 D(I)=D(I)-B
440 NEXT I
450 B=ABS(B)
460 PRINT\PRINT\PRINT
470 REM FIND MAX. DATA VALUE
480 T=0
490 FOR I=1 TO N
500 IF T<D(I) THEN T=D(I)
510 NEXT I
520 REM PLOT DATA
530 S=L/T
540 E=S*B
550 PRINT\PRINT
560 PRINT "    DATA PLOT (NORMALIZED)"
570 PRINT\PRINT
580 PRINT "X1= ",X1
590 GOSUB 1190
600 FOR I=1 TO N
610 IF S*D(I)<1 THEN GOTO 620
620 IF S*D(I)<1 THEN PRINT "*"
630 IF S*D(I)>=1 THEN PRINT TAB(S*D(I)),"*"
640 IF S*B<1 THEN GOTO 660
650 PRINT TAB(E),":"
660 NEXT I
670 GOSUB 1200
680 PRINT "X2= ",X2
690 REM START FOURIER TRANSFORM
700 DIM F(N)
710 FOR I=1 TO N
720 W=(I-1)*W3
730 C1=0\S1=0
740 FOR M=1 TO N
750 X=X1+(M-1)*D
760 G=W*X
770 C1=C1+D(M)*COS(G)
780 S1=S1+D(M)*SIN(G)
790 NEXT M
800 F(I)=SQRT(S1*S1+C1*C1)*D
810 IFI=1 THEN GOSUB 1260
820 NEXT I
830 REM END FOURIER TRANSFORM
840 PRINT\PRINT
850 REM TRANSFORM DATA TABLE
860 PRINT "   FREQ(RAD)   MODULUS"
870 PRINT "   ---------   -------"
880 FOR I=1 TO N
890 PRINT "     ",INT(1000*W3*(I-1)+.5)/1000,
900 PRINT "    ",INT(1000*F(I)+.5)/1000
910 NEXT I
920 PRINT\PRINT
930 REM TRANSFORM PLOT
940 PRINT "    FREQUENCY PLOT (NORMALIZED)"
950 PRINT\PRINT
960 PRINT INT(1000*W1+.5)/1000,
970 PRINT " RADIANS/SECOND    ",
980 PRINT INT(500*W1/3.141595+.5)/1000,
990 PRINT " HERTZ (CYCLES/SECOND)"
1010 GOSUB 1200
1020 T=0
1030 FOR I=1 TO N
1040 IF T<F(I) THEN T=F(I)
1050 NEXT I
1060 S=L/T
1070 FOR I=1 TO N
1080 IF S*F(I)<1 THEN GOTO 1090
1090 IF S*F(I)<1 THEN PRINT "*"
1100 IF S*F(I)>=1 THEN PRINT TAB(S*F(I)-.5),"*"
1110 PRINT ".",TAB(L-1),"."
1120 NEXT I
1130 GOSUB 1200
1140 PRINT INT(1000*W2+.5)/1000,
1150 PRINT " RADIANS/SECOND    ",
1160 PRINT INT(500*W2/3.141595+.5)/1000,
1170 PRINT " HERTZ (CYCLES/SECOND)"
1180 END
1190 REM BOARDER LINE PLOT
1200 FOR I=1 TO L
1210 PRINT "*",
1220 NEXT I
1230 PRINT
1240 RETURN
1250 REM CORRECT DC VALUE FOR DATA SHIFT
1260 C1=C1-N*B
1270 F(1)=ABS(C1)*D
1280 RETURN
READY
```

number of data points, *N*, as initial inputs. It then asks for a frequency scale factor (to be discussed shortly). After receiving this information it then asks for the *N* data values, f_i. These are plotted, and the computer subsequently enters the Fourier transform calculation, which may take several minutes. At the end of this calculation, the *N* frequency data points are printed out. This is where the effect of the frequency scale factor becomes evident. With a scale factor of unity, the Nyquist sampling criterion is used to determine the maximum frequency to be used in the transform calculation. The frequency range is divided into *N-1* intervals, and the frequency space data points are plotted at the associated *N*

```
***FOURIER SPECTRUM ANALYZER***

THIS PROGRAM TRANSFORMS EQUAL INCREMENT DATA INTO
FREQUENCY SPACE

THE USER INPUTS THE STARTING AND ENDING COORDINATES,
ALONG WITH THE NUMBER OF DATA POINTS THE PROGRAM WILL
THEN PLOT THE DATA AND ITS SPECTRUM

INPUT TERMINAL WIDTH: ?51
BEGINNING COORDINATE: ?0
ENDING COORDINATE: ?6.28
NUMBER OF DATA POINTS: ?17
INPUT SCALE FACTOR: ?1
INPUT DATA
   1?0
   2?.38
   3?.71
   4?.92
   5?1
   6?.92
   7?.71
   8?.38
   9?0
   10?-.38
   11?-.71
   12?-.92
   13?-1
   14?-.92
   15?-.71
   16?-.38
   17?0
```

Figure 1: *Initializing routine for a seventeen-point approximation of a one-period sine wave. The period chosen was 2π. Thus, the characteristic frequency associated with this sine wave is one radian per second.*

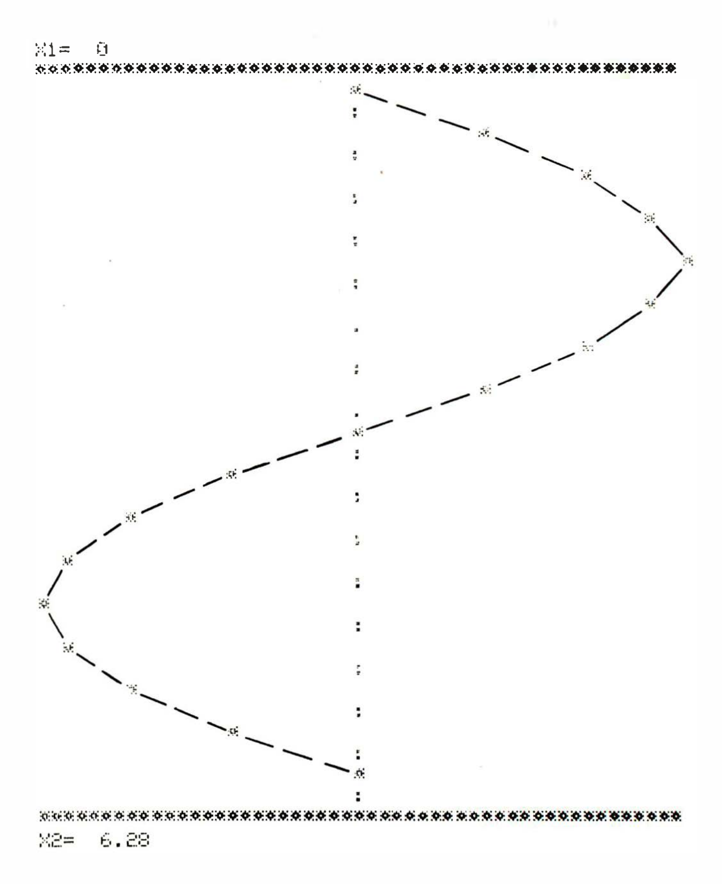


Figure 2: *Computer responds with a plot of the data set. For added clarity, lines have been drawn between the plotted points on this and all subsequent figures.*

boundaries. With an inputted scale factor greater than unity, the maximum frequency is reduced correspondingly. This gives better resolution for examining low frequency components. Scale factors less than unity are not permitted.

A sample run for a seventeen-point approximation of a single period of a sine wave is shown in figures 1, 2, and 3. We expect to see no "power" at $w=0$ on the frequency plot because the average value of the data set is zero. Such is the case, since the signal approximated is a discrete truncation of a continuous sine wave having a frequency of one radian per second. However, because the wave has been truncated, there are many other frequency components present which not only spread out the power around the one radian per second point, but also appear to shift the frequency spectrum maximum towards a lower frequency. The same features are apparent in figure 4 where the frequency resolution has been increased three-fold.

Truncated Sine Waves

The plots presented in the last section demonstrated that, although we intuitively expect a peak in the frequency spectrum at the sine wave frequency, none is apparent. If figure 4 is viewed with a little imagination, however, it is possible to see that the complete spectrum is composed of two parts, with one part having a peak at the sine wave frequency, thus causing the small bump at $f = 1$ radian per second in figure 4.

Since we have a computer program that allows easy evaluation of frequency spectra, consider the approximate square-wave data set shown in figure 5. The corresponding frequency plots are shown in figures 6 and 7. Mathematically we expect to see a "sinc" function, ($F(z) = \sin z/z$), frequency response, with the exception of having a zero at $w=0$. The next zero is expected to be at 2 radians per second. From the frequency plots we see the expected characteristic shape, but with a zero at 1.9 radians per second; the input square wave is not ideal. A direct comparison of figures 3, 4, and 6, 7 indicates that the single-period sine wave has a spectrum similar to that of the single-period square wave, with the important difference that there appears to be more high frequency content in the square-wave spectrum. This is not surprising since there are sharp edges in the square-wave truncation which should lead to more high frequency components than with the sine-wave truncation.

Since the spiked-spectrum characteristic of an infinitely long wave is not very evident in the single-period wave truncation example given above, the question arises: how many sine wave periods are required before the frequency content that is characteristic of the single-period square wave is sufficiently reduced to allow the spiked spectrum to become evident? Again, we can experiment using the computer by entering a thirty-three data point representation of a two-period sine wave and observing the resulting frequency plot (see figure 8). As expected, the infinite sine-wave characteristic is much more evident

FREQ(RAD)	MODULUS
0	0
.5	4.778
1.001	3.16
1.501	2.076
2.001	.392
2.501	.84
3.002	.392
3.502	.522
4.002	.392
4.502	.35
5.003	.393
5.503	.232
6.003	.392
6.503	.149
7.004	.393
7.504	.079
8.004	.393

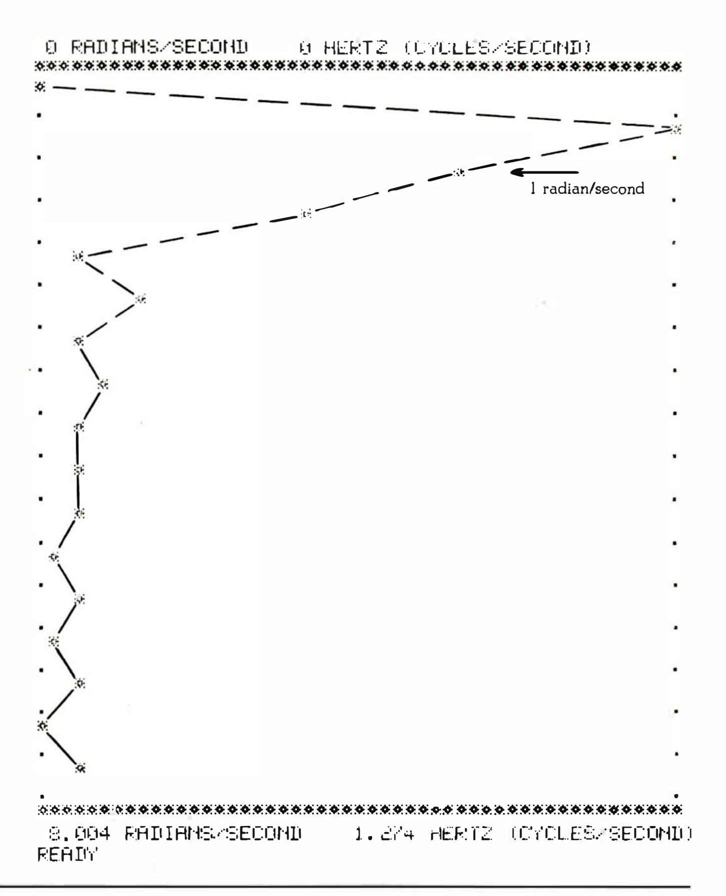


Figure 3: *The program outputs a table of transformed data, as well as a frequency space plot.*

because the term which appears to be related to the truncation has collapsed two-fold in the frequency span.

To those familiar with Fourier transforms of signals which have been "windowed," the first low frequency zero shown on figure 8 (other than that at $w = o$) is directly related to this "window function." This function may be considered as multiplying an infinite sine wave to give the observed truncation, thus the frequency spectrum of the resulting signal is the convolution (see convolution theory in *The Fast Fourier Transform* by Brigham) of the perfect sine wave spectrum with the spectrum of this window function, the latter having a functional form defined by (F(z) = sin z/z). As the window becomes relatively

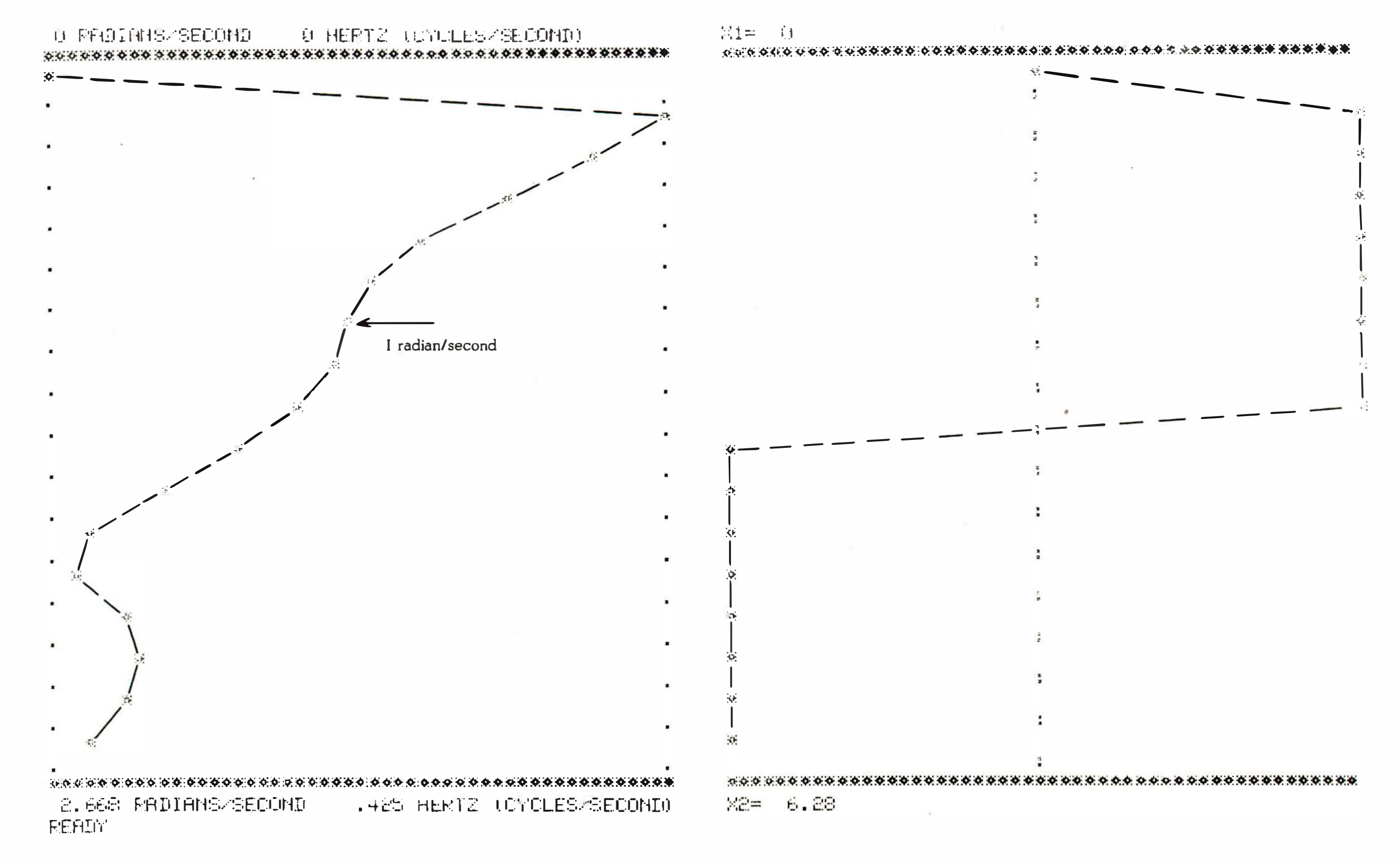


Figure 4: *Same frequency plot as shown in figure 3, but with a 3.0 scale factor condition (three-fold increase in frequency resolution).*

Figure 5: *Plot of the seventeen-point data set used to approximate a square wave having the same period as the sine wave examined in figures 2 and 3.*

wider,the sine function increasingly takes on a delta (or impulse) function characteristic which eventually leads to a spiked spectrum for the resulting transform. Figures 9 and 10 demonstrate this for approximations of four- and eight-period sine waves. The latter plot definitely shows the narrow band spectrum element that is expected for a sine wave. Note, however, that the spread in power around the sine wave frequency still remains.

Frequency-Shift Keying

One of the techniques used to encode digital information for transmission or recording is frequency-shift keying (FSK). In this method a frequency f_o is associated with the logic state 0, and a frequency f_1 is associated with the logic state 1. Thus a message consists of a sequence of sine wave bursts, each having a characteristic frequency f_o or f_1. It is apparent that the ideas and plots developed in the previous section may be directly applied to the consideration of FSK encoding.

If the data-signal center frequency is 2100 Hz (which is equal to $(f_o + f_1)/2$), and if the desired data-transfer rate is 300 bits per second, then one may expect to see (and subsequently decode) many bursts of seven-period sine waves having frequency spectra similar to that shown in figure 10, though scaled in frequency. Obviously, if the two chosen encoding frequencies are very close together it will be difficult to reliably sort out the signals using a filter technique. If a linear filter approach is taken, then it is apparent by examination of figure 10 that a minimum frequency separation of about $(f_o + f_1)/8$ is called for. For a 2100 Hz center frequency, a 500 Hz frequency separation is required. This gives encoding frequencies of approximately 1850 and 2350 Hz. More will be said about the significance of those frequencies later.

The above frequency separation requirement was obtained by considering several factors. These considerations included the decoding technique, filtering, and determining whether or not the frequency spectra are sufficiently separated to allow filter detection (using many dB per octave roll off). Another approach, which is more accurate, is to count sine wave periods or zero crossings. If periods are used, the minimum required frequency separation is that which gives a one-period difference (eg: seven periods versus eight periods). In this case, the required frequency separation comes out to be 300 Hz. This can be reduced to 150 Hz using zero crossings. To get better discrimination than this, a technique such as phase-locked loops must be used, and the results are highly hardware-design dependent.

For the sake of comparison, consider some of the frequencies used in the real world. The standard modem frequencies are separated by 200 Hz; 2025/2225 Hz and 1070/1270 Hz. For standard modem encoding frequencies, you must do more than simply decode by filtering.

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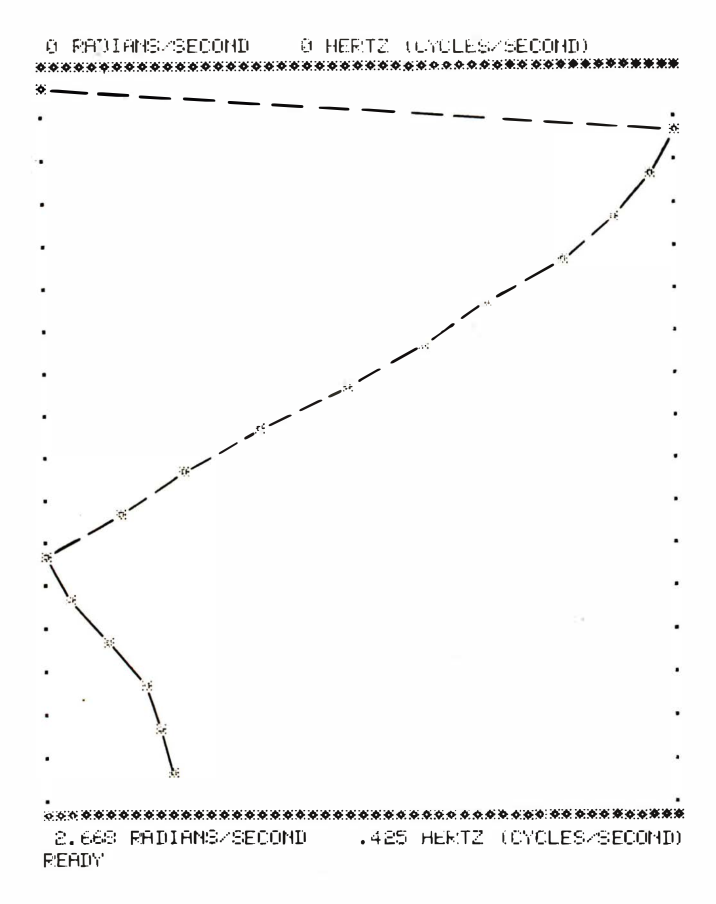


Figure 6: *Frequency space plot of the square wave approximated by the seventeen-point data set shown in figure 5.*

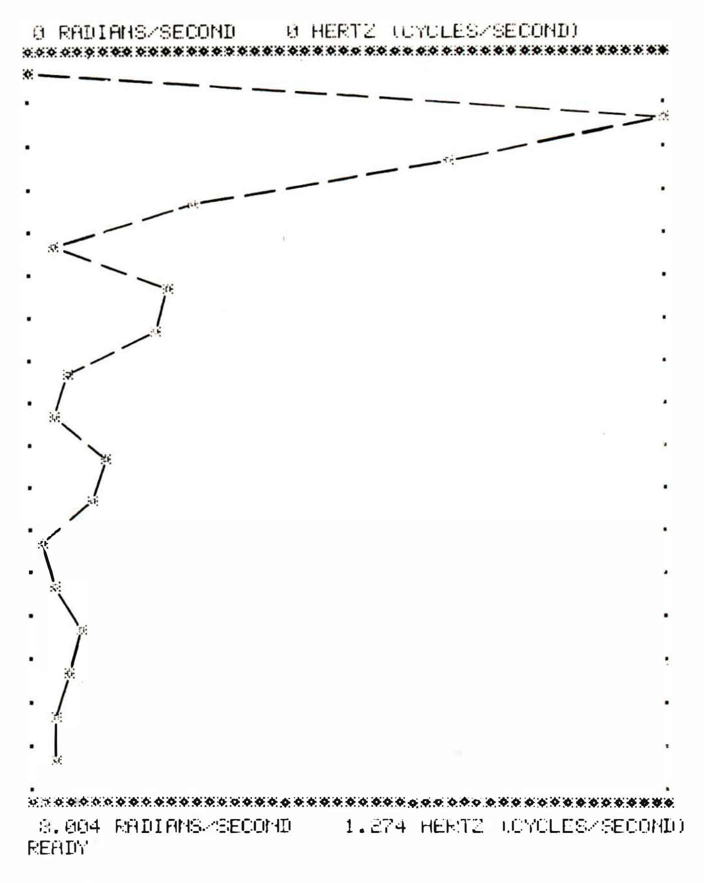


Figure 7: *Same waveform as in figure 6, but with a frequency scale factor of 3.*

The MITS 88-ACR audio cassette record interface was originally designed to work at the upper modem frequencies. Difficulty in reliability ensued, and the two frequencies were subsequently changed to 1850 and 2400 Hz. These frequencies are curiously close to those that were derived from the frequency spectrum separation consideration above, and perhaps indicate that the 88-ACR has a poorly operating phase-locked loop combined with some tape flutter. This suspicion is based on the fact that the 88-ACR center frequency is derived from a control voltage which is obtained from dividing down a power supply voltage. Therefore, supply noise/ripple can cause trouble.

One cassette interface board exists which is advertised as able to use preset filters for decoding. Its encoding frequencies are 1200 and 2400 Hz. From figure 9 (four-period sine wave) and figure 10 (eight-period sine wave) it is apparent that sufficient separation should exist between the 1200 Hz signal spectrum (which is the troublemaker; large spread plus harmonics) and the 2400 Hz spectrum to allow for reliable filter detection.

The above has demonstrated how, with a little experimentation using the Fourier transform program, insight can be gained into some important communications principles without going deeply into mathematics.

Noise

In the laboratory the situation will often arise in which the signal of interest is buried in noise. In this section we consider an example in which an eight-period raised sinusoid is covered by uncorrelated noise having roughly the same amplitude as the sine wave. Figure 11 shows a 65 point approximation to a raised sine wave packet having the following form:

$$f_i = 2 + sin(x_i) \quad (7)$$

The data set may be conveniently generated by insertion of the following statements into the program shown in listing 1:

```
181    X1 = 0
182    X2 = 50.3
183    N = 65
184    FOR I = 1 TO N
185    D(I) = 2 + SIN ( (I-1)*X2/(N-1) )
186    NEXT I
187    GOTO 250
```

The corresponding frequency space plot is shown in

Text continued on page 26

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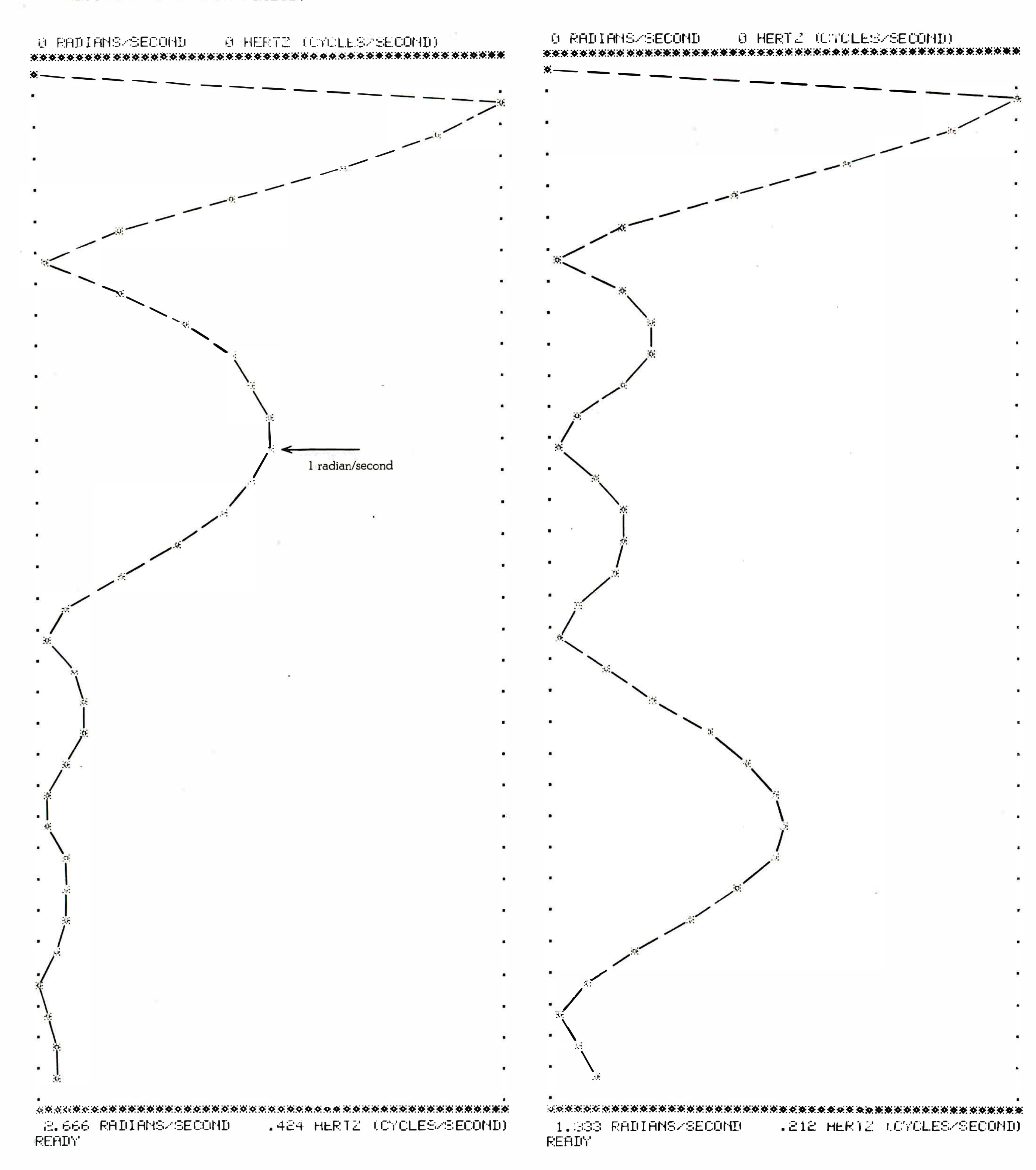


Figure 8: *Frequency plot of a two-period sine wave approximated by a thirty-three-point data set. A frequency scale factor of 3 was used.*

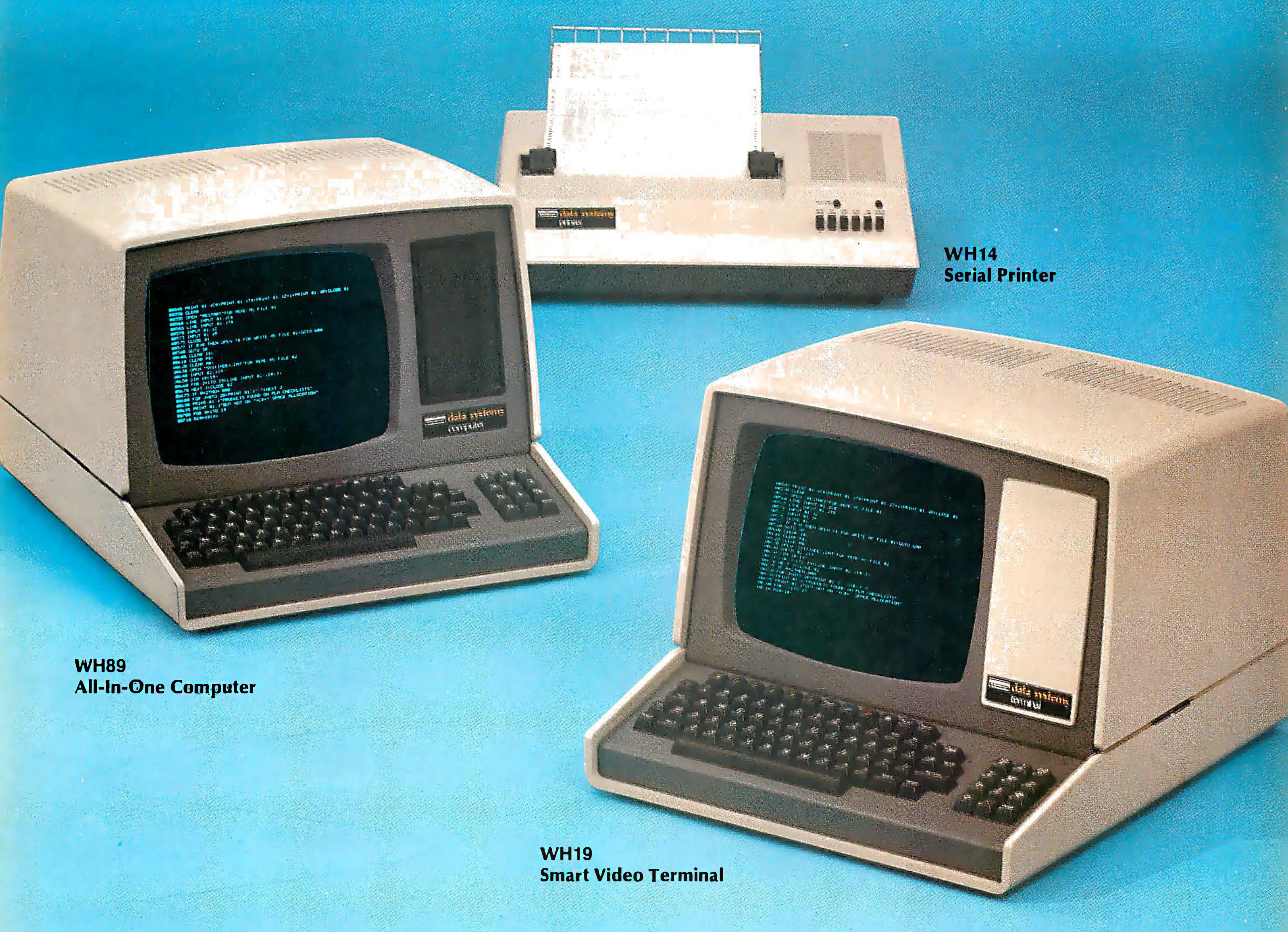
Figure 9: *Frequency space plot of a four-period sine wave approximated by a thirty-three-point data set. A scale factor of 3 was used.*

Text continued from page 22:
figure 12. Observe that there is a large value at $w=0$ which dwarfs the power at the characteristic sine-wave frequency. A high pass filter would remove the $w=0$ term.

Figure 13 shows the effect of adding uncorrelated noise to the above sine wave via the following formula:

$$f_i = 2 + \sin(x_i) + 2\{RND[(I-1)/(N+1)] - 0.5\} \quad (8)$$

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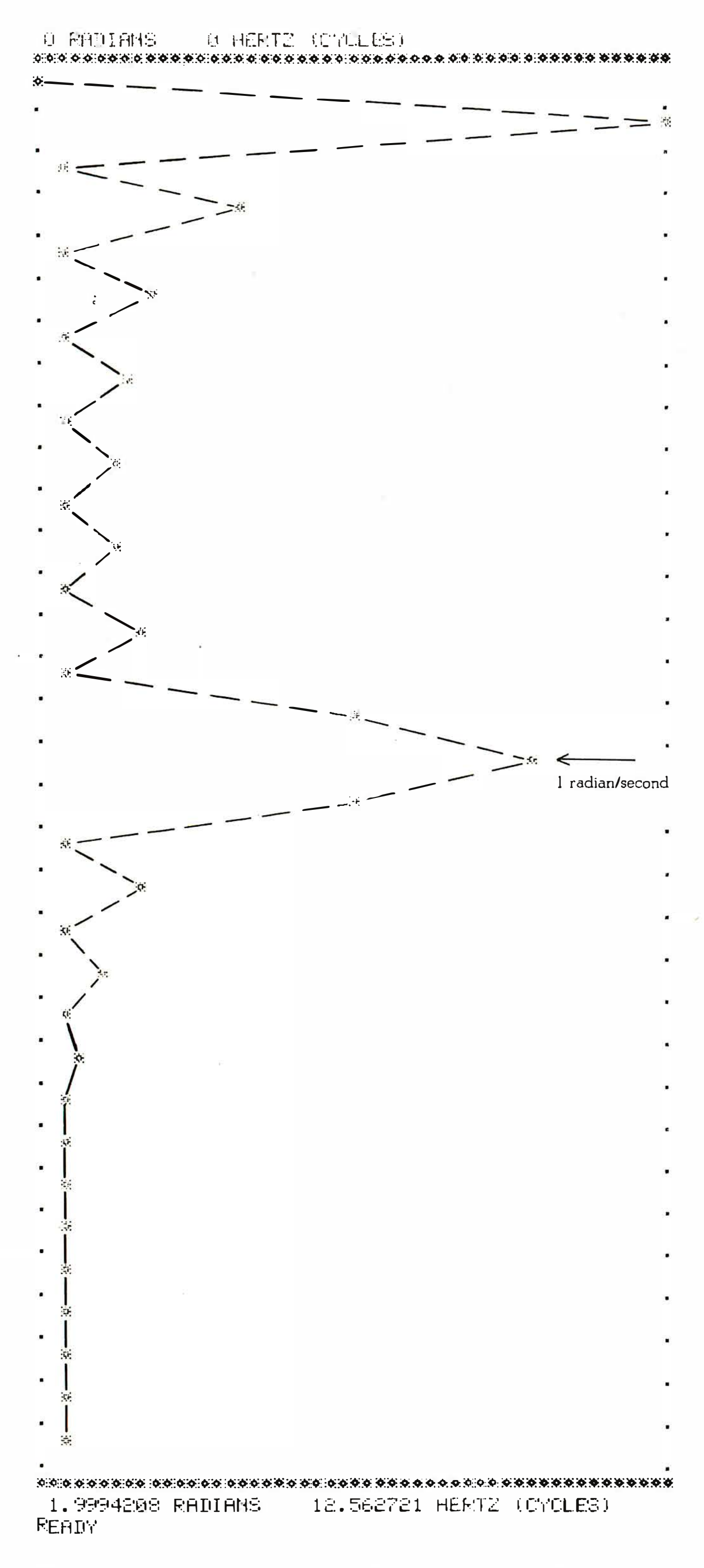


Figure 10: *Frequency space plot of an eight-period sine wave approximated by a sixty-five-point data set. Normal resolution.*

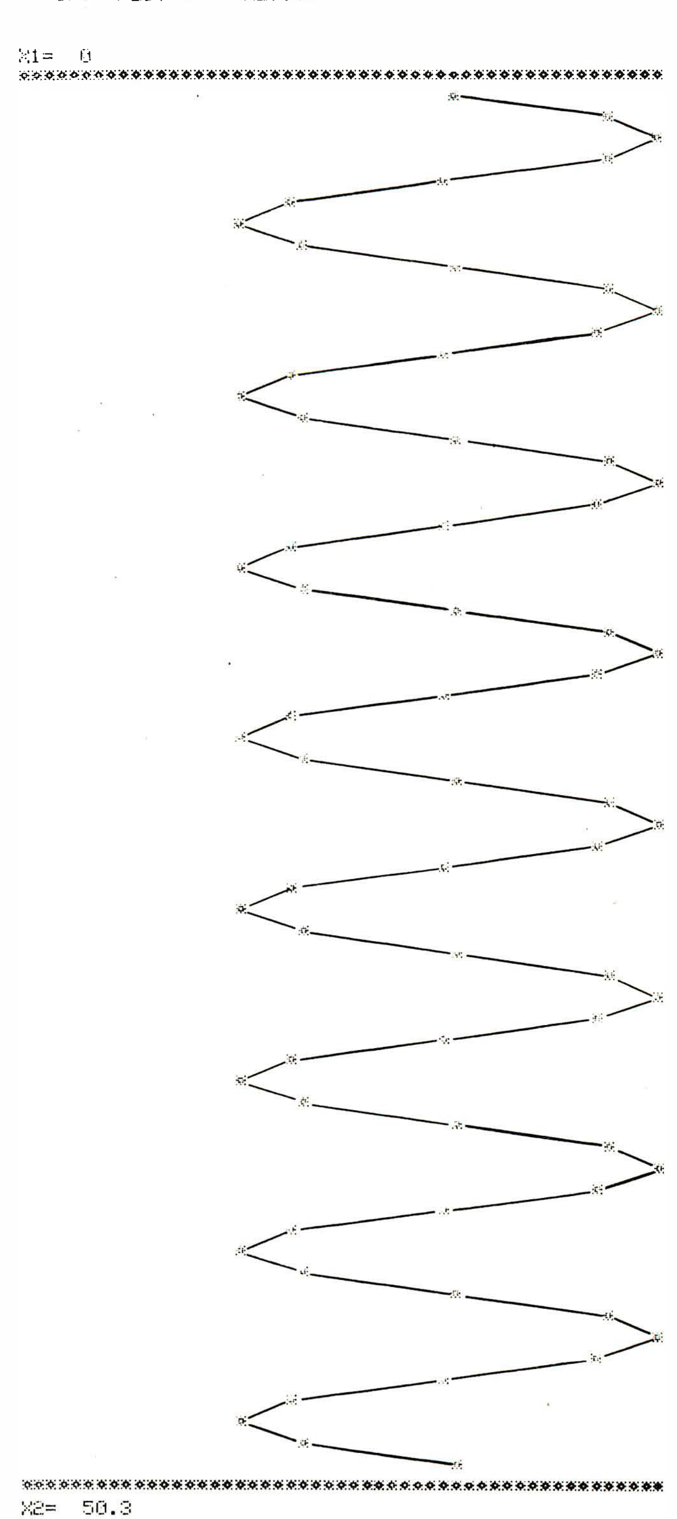


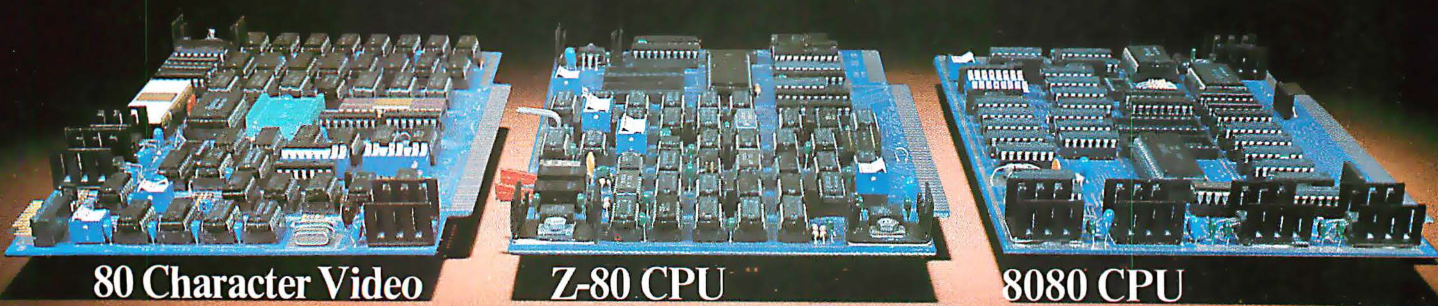
Figure 11: *Eight-period sine wave as approximated by a sixty-five-point data set.*

Observe that the average value of the noise is zero and that the noise added is uncorrelated because a new "seed" for the random number generator is chosen at each data point. This noise is not "white" or Gaussian, but rather is linearly distributed between -0.5 and +0.5.

The sine wave hidden in figure 13 is not very evident, although you might guess (perhaps from an oscilloscope trace) that a repetitive signal is present.

Figure 14 shows the frequency transform of the noisy data from figure 13. Observe that, although there is noise

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CB2 also features an MWRITE signal, firmware vector jump, and an output port to control 8 extended address lines (allowing use of more than 65K of memory). Jumper options generate the new IEEE S-100 signals to insure future S-100 compatibility.

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8080 CPU

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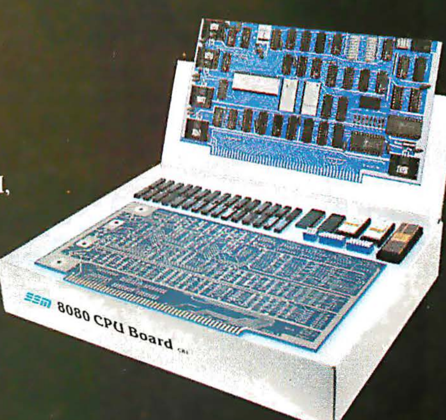
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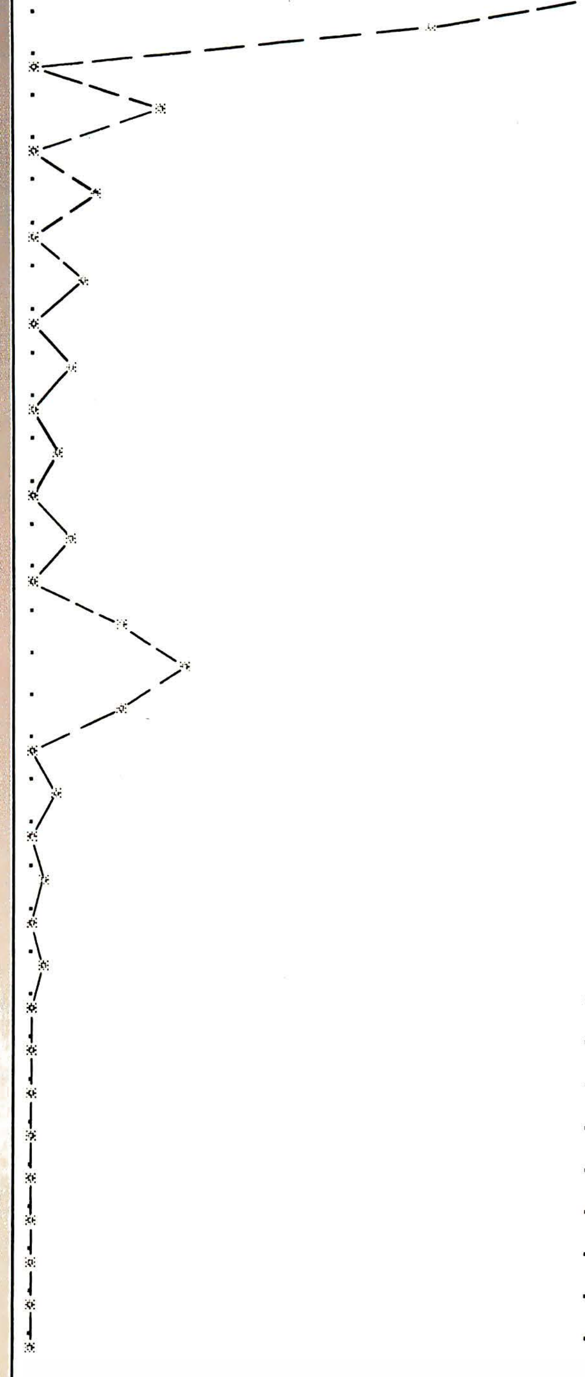


Figure 12: *Frequency space plot of a raised eight-period sine wave as approximated by a sixty-five point data set.*

in the frequency spectrum, the sine wave component is clearly evident. Thus, to recover information about the amplitude of the sine wave component, you could use a narrow band filter to look at the spectrum content in the vicinity of the sine-wave characteristic frequency. Using Gaussian noise in this example gives much the same result.

Noisy data sets, as above, can be created (us-



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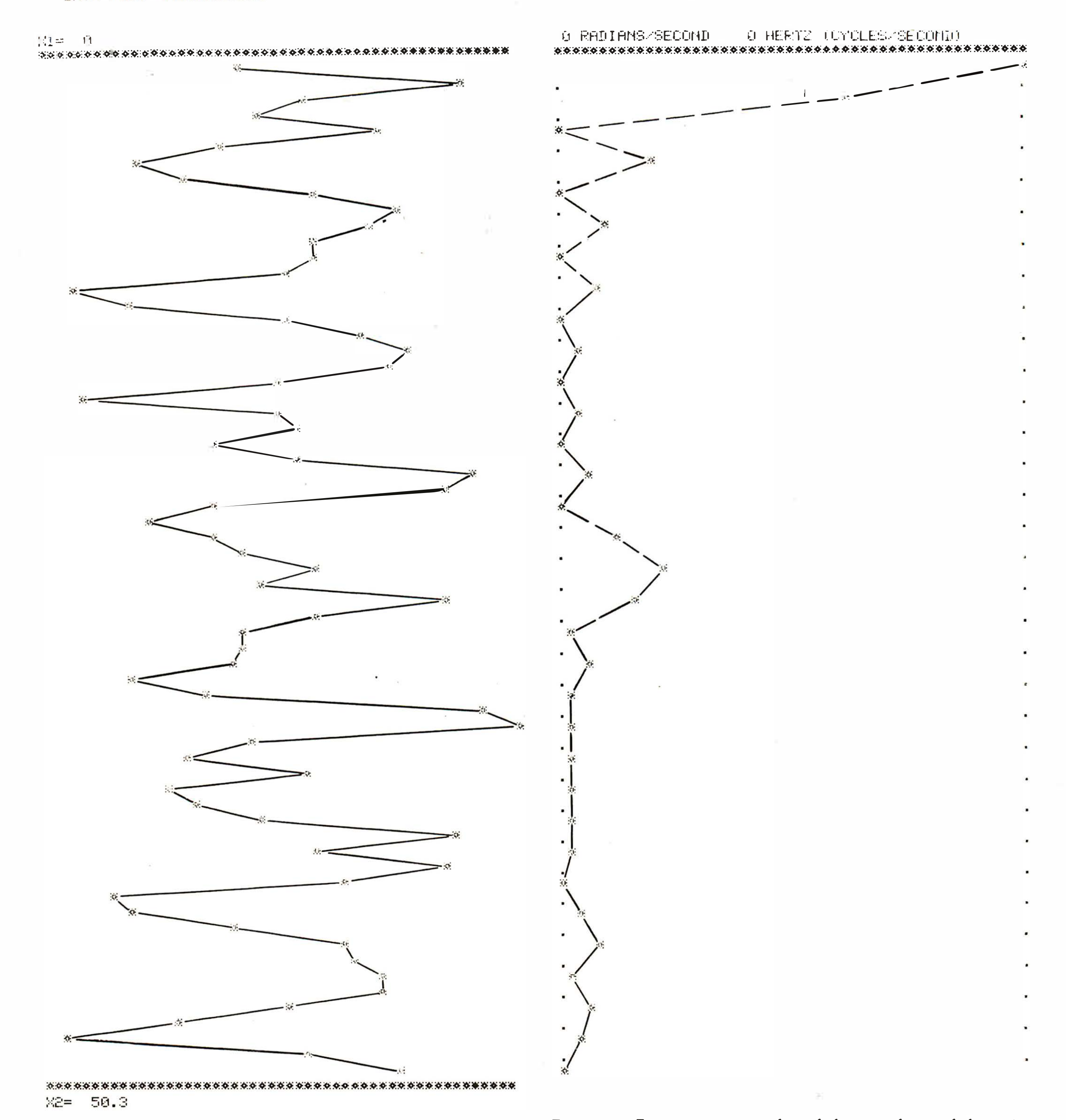


Figure 13: *Same waveform as in figure 11, but with noise added.*

Figure 14: *Frequency space plot of the transform of the noisy data set shown in figure 13.*

ing a Gaussian noise distribution) many times. If this is done each time using new random number generator seeds so that there is no correlation between data sets, then the noise will on the average appear to be uniformly distributed along the frequency axis. At the sine-wave frequency that I have chosen, you can expect to see an average noise *power* ($|F_n(w)|^2$) of some value N_8. If we measure the *power* ($|F_s(w)|^2$) at the sine-wave frequency, we can expect to see an average value S_8. The amplitude signal to noise ratio (S/N) is then:

$$(S/N)_8 = S_8/N_8 \qquad (9)$$

If we had instead looked at a sixteen-period raised sine wave having the same characteristic frequency and the

same impressed noise level, the average noise *power* would have been twice as great, or $N_{16} = 2N_8$. This conclusion is based on the *noise power* × *time* product. The total *energy* in the sine wave component (the energy in the bump at w = one radian per second) also doubles. However, we have seen in the previous examples that the width of the sine-wave component narrows as the number of periods increases (width in frequency space is proportional to the inverse of the number of periods). Thus, the power at the characteristic frequency for the sixteen-period sine-wave quadruples, or $S_{16} = 4S_8$. The power signal to noise ratio is:

$$(S/N)_{16} = 2\ (S/N)_8 \qquad (10)$$

It can be shown that by increasing the length of the sine wave sampled by a factor n you can improve the *amplitude S/N* by $\sqrt{n}$. (Lock-in amplifiers can also be used to improve S/N. Observe that increasing the sampling time is analogous to including more periods; S/N is proportional to $\sqrt{sampling\ time}$, or $1/\sqrt{bandwidth}$.)

Conclusion

The computer program presented in listing 1, although not optimal in efficiency, is reasonably universal and capable of being used in many applications. The application considered above was the evaluation of frequency-shift keying encoding method, in terms of decoder bandwidth, band separation, and noise immunity.

A simple extension of the program could be implemented by generating the phase component of the complex frequency spectrum. This can be done by placing another few statements in the program:

```
Insert: 805 P(I) = ATAN (S1/C1)
Add: DIM P(I), print and plot routines
```

P(I) represents the phase in radians. Since North Star BASIC, Version 6, Release 2 does not have the inverse tangent function, an additional subroutine for calculating the inverse tangent would be necessary. For the examples given above, the phase response was not an important consideration, and would have increased the computing time.

The use of the complete transform, both amplitude and phase, encourages some interesting experiments in the realm of signal recovery. For example, a low resolution signal (eg: an image scan such as that from an analog bar-code reader) could be transformed, and the resulting transform could be corrected for the device response. The resulting corrected transform could then be retransformed back into signal (optical image) space. This is particularly easy (and effective) when the device response is stable and there is sufficiently little noise. For example, with a simple optical device such as a grocery store bar-code reader, the unaided resolution in terms of edge response may be on the order of 0.005 inches. With correction this can be improved to 0.0005 inches, an order of magnitude improvement in edge response. Such corrections are not uncommon as most quality tape recorders have playback frequency compensation. In the latter case, an analog circuit is used instead of a computer.

The preceding resolution improvement approach is based on the assumption that the system being considered is linear. Optical systems are convenient in this respect, and much can be done with the transforms of optical images—witness the Mariner photos. The program presented here offers the opportunity to experiment with some of these techniques. ■

REFERENCES

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A Dictionary of Microcomputing, Philip E Burton, Garland Publishing Inc, 1976.

Glossary

center frequency: 1. *The mean frequency of the output wave when modulated by a symmetrical signal.* 2. *The center frequency in a frequency spectrum plot.*

harmonic distortion: *The production of undesirable harmonic frequencies at the output, due to circuit nonlinearities when a sinusoidal voltage is applied to the input.*

Fast Fourier Transform: *(FFT) A mathematical concept that describes the relationship between information in the time domain and the frequency domain. The Fourier transform of correlation functions will yield the power spectra.*

flutter: *The variations in frequency caused by irregular motion of the recording device during the recording process. Flutter usually refers to high-frequency variations, and the term "wow" denotes low-frequency deviations.*

frequency compensation: *A technique involving modification of a circuit to improve the linearity of its response with respect to frequency over the existing bandwidth.*

frequency response: 1. *A measure of how effectively a circuit or system transmits the different frequencies that are applied to it.* 2. *The section of the frequency spectrum which can be sensed by a device within specified amplitude error tolerances.*

frequency-shift keying: *(FSK) A method of frequency modulation that involves shifting the output frequency between predetermined values corresponding to the frequencies of correlated sources.*

frequency spectrum: *An entire range of the distribution of the intensity of an electro-magnetic or acoustic radiation as a function of frequency.*

noise immunity: *A measure of how sensitive a circuit is to electrical interference or other sources of noise.*

overshoot: 1. *An initial transient response to a unidirectional variation in input which exceeds the steady state response.* 2. *The maximum amount by which this transient response exceeds the 100% amplitude level.*

phase-locked loop: *A circuit which compares the input carrier frequency with the frequency of the voltage*

controlled oscillator (VCO) by means of a phase detector; the ouput of the phase detector is fed through a loop filter and then back to the voltage controlled oscillator to keep in phase with the incoming carrier frequency.

phase shift: 1. *The difference between corresponding points on the input and output signal waveforms, commonly referred to as the phase angle.* 2. *A change in the phase angle between two periodic signals.*

processor: *(CPU — central processing unit) The central control unit of the digital computer. This unit contains the memory, the Arithmetic and Logic Unit (ALU), control circuitry, and general purpose registers. The processor controls the decoding and execution of all machine instructions.*

real-time operation: *A computer mode of operation in which the input data is received and processed as it is generated so that the current information may be used to control that process.*

rise time: *The time required for the leading edge of a pulse to rise from 10% to 90% of its steady-state value. It is proportional to the time constant and is a measure of how quickly the signal makes a transition form one state to another.*

signal-to-noise ratio: *(S/N ratio) A measurement of the relative quality of a signal. Precisely the ratio of the magnitude of the signal to the magnitude of the noise present.*

video display: *(CRT — cathode ray tube) a peripheral which presents its data visually on a television-like screen.*

Add Nonvolatile Memory to Your Computer

Steve Ciarcia
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"You know, Ray, sometimes I think I see more of you than your wife does."

He grinned and retorted, "I just dropped over to see what the Circuit Cellar Frankenstein was cooking up this month."

I fully deserved that. Few have seen the Circuit Cellar, and it does look a little imposing at first. The usual 20-square-foot hobby corner used by most computerists has been expanded to a 1000-square-foot computer room which vaguely resembles the bridge of the starship *Enterprise.* Accented with the eerie appearance of seven video displays and a multitude of strange black boxes emanating menacing sounds, it sometimes becomes an environment of computerized insanity. While I am not interested in creating any monsters, Baron von Frankenstein and I may have a few interests in common. His demise, I assure you, was simply a case of bad press.

"Steve?" Ray said loudly. "What are you working on?"

I was jerked back to reality somewhat abruptly. Visions of a 1932 movie set faded as I turned in my swivel chair to respond.

"I am actually working on several ideas, Ray, but the easiest is trying to put a computer in a car."

Ray quickly cast a doubtful glance at the 64 K-byte, dual-disk, Z80-based system. Returning his attention to me he quipped, "Where do you plan to put the printer?"

"I do not mean a big computer. I mean a little one, probably a single board. I will have sensors throughout the car to monitor engine speed, temperatures, pressures, and so forth fed to a display visible to the driver. The driver will be able to calculate and keep running totals of gas mileage, monitor the engine performance, and generally maintain a comfortable feeling of safe motoring."

Ray said, "That sounds pretty good. You will obviously have to use CMOS for your computer." His observation was based on his long years of technical experience.

"Why?"

Ray seemed confused at my reply. He expected agreement. Shouldn't complementary-metal-oxide semiconductor (CMOS) components be used since the computer will be battery powered?

"Because it is battery powered. That's why!" he demanded.

"That is not necessarily true." Trying not to seem quarrelsome, I continued. "Let's think about an automobile for a minute. There are many power-consuming devices. A defroster fan or rear-window heater can draw 100 watts each. Without the floppy-disk drives, even that big Z80 system over there does not pull that much. I am shooting to stay under 20 watts, but logic type does not make much difference."

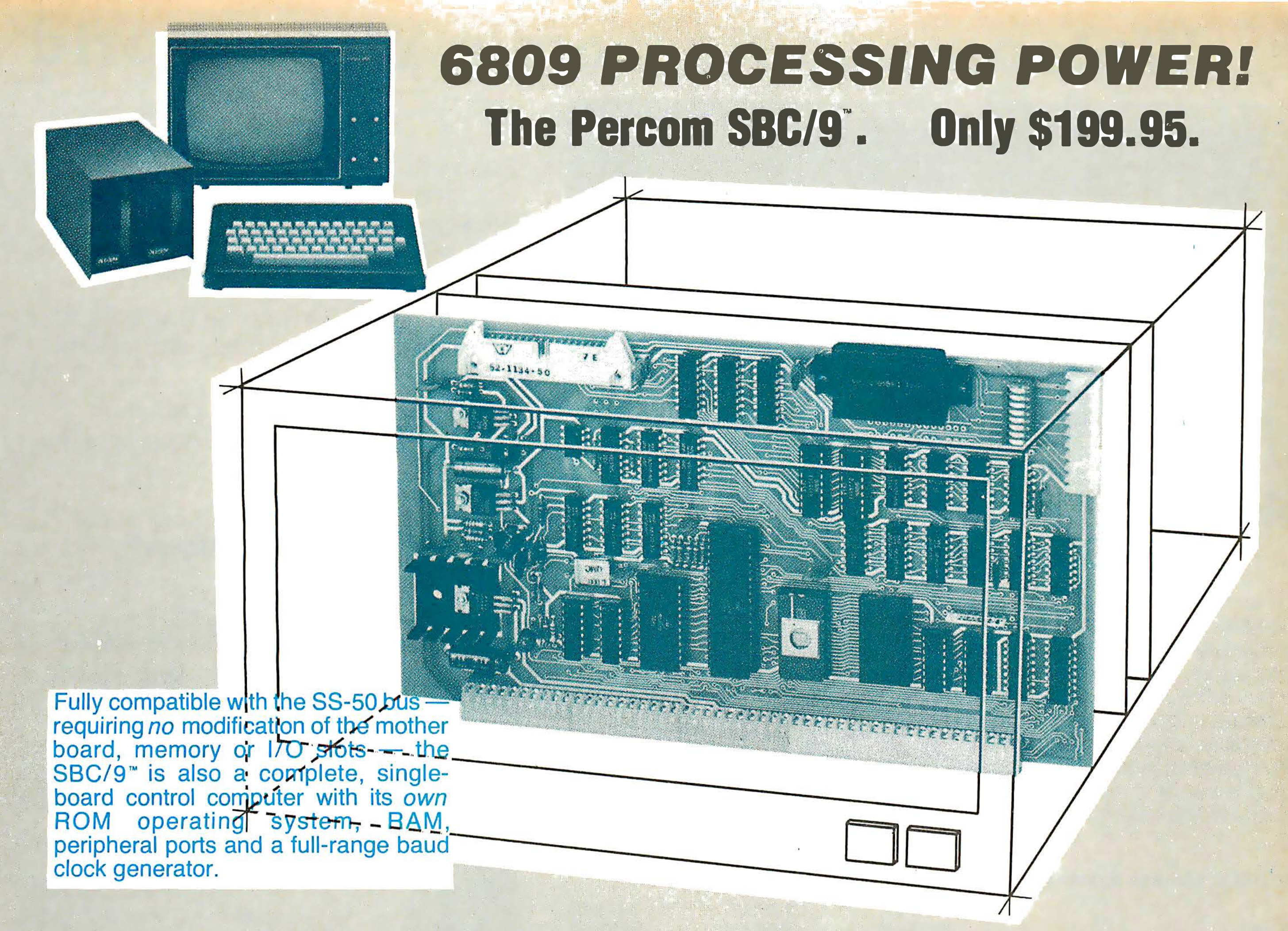
"Yes, I know when the engine is running there is plenty of power available from the alternator." Ray seemed a bit frustrated in pointing out my misjudgement of the facts. He persisted. "At 12 volts, 20 watts is almost 2 amperes! The 12-volt car battery will not last long with the engine off."

"You do not leave the defroster fan on with the engine off, do you?" I countered.

"Of course not! But what about your program? If it is written into programmable memory such as 2102 or 2114 devices, you'll lose it when the power goes off."

"I said this computer is for automotive use. It cannot be considered as a general-purpose computer. Rather than using only programmable memory with programs loaded from tape or disk, it will have the operating system and language interpreter stored in read-only memory and application software stored in erasable, programmable read-only memory, an EPROM. The only programmable memory needed will be a

Text continued on page 40



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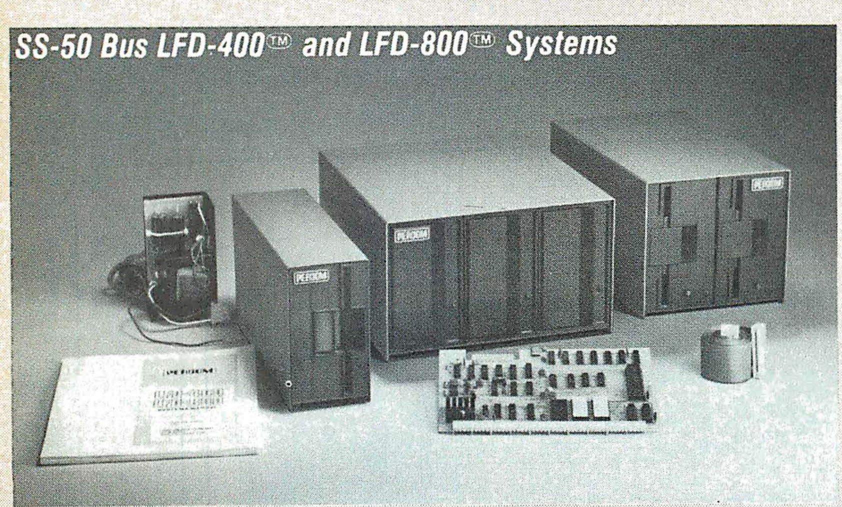
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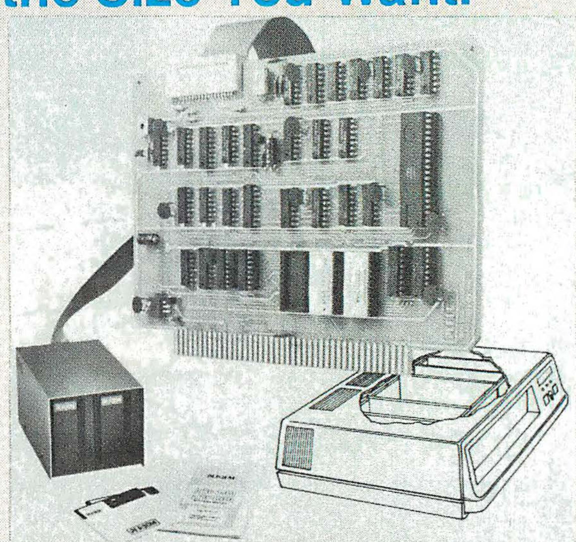
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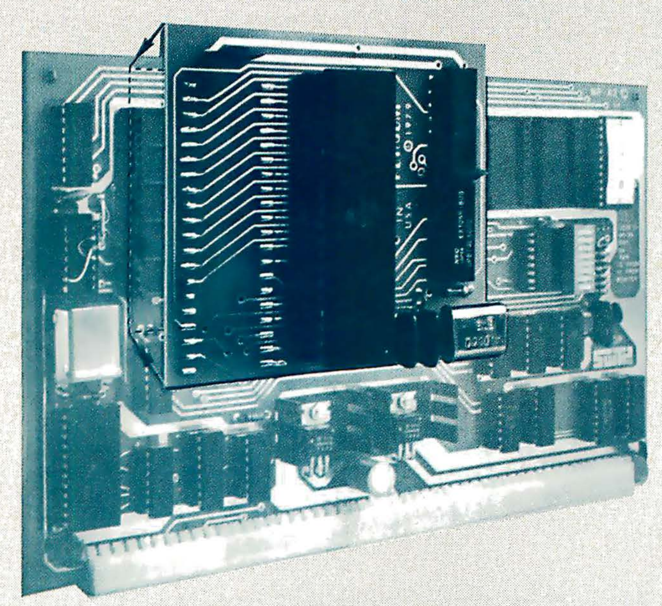
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of 6800 Microcomputing.

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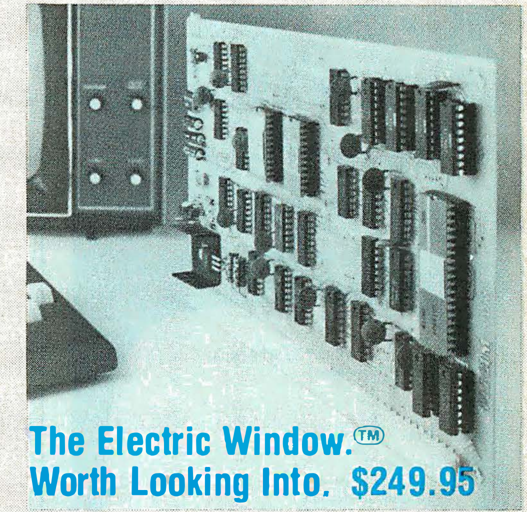
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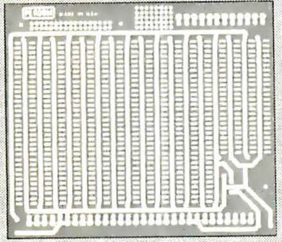
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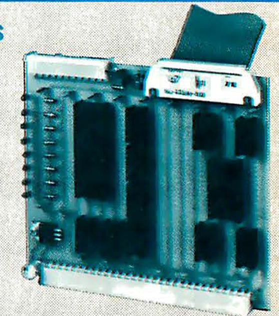
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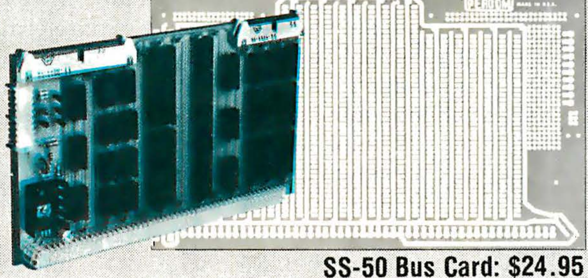
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Text continued from page 36:

scratch pad for calculations and a small area set aside for storage of continually updated, long-term quantities like mileage and gas consumption."

Ray was not incorrect. The language interpreter and application program *could* reside entirely in programmable memory as in most older personal computers. Memories composed of 2102A devices can, in fact, be put in a stand-by mode by dropping the power-supply voltage to 2 V. This reduces power consumption by 80% while still retaining data.

While being practical under most circumstances, stand-by operation is not a total solution. Depending upon the system configuration, memory power might have to be sequenced on and off, and perhaps be isolated from the 5-V supply of the rest of the system.

The ultimate value of this technique is dependent on efficient power conversion. A 12-V-to-2-V converter with 50% efficiency would be self-defeating. Battery power, however much reduced, is still required as long as memory data is to be retained.

Hybrid computers exist wherein high-speed, bipolar microprocessors are mated with low-power CMOS memory. Such a system could have various forms of read-only memory as before, but in the form of complementary-metal-oxide devices rather than bipolar memory chips.

Data retention time would probably be an order of magnitude longer, but there are complications associated with mixing logic families. All things considered, if it were not for the high cost of CMOS memory, I would use it.

Ray persisted, saying, "You still have to provide continuous power for *some* programmable memory if you intend to store those long-term values." Ray was convinced that I must have constant power on something. I hated to disillusion him.

I explained, "Not necessarily. I considered the usual standby-mode programmable memory, both CMOS and bipolar types, and rejected them. Bipolar standby takes too much power; and CMOS memory chips might be destroyed by physical handling. This is experimental, you know."

Ray said, "If you intend to shut off the computer entirely, then I suppose you could write out data to an audio cassette to be reloaded when you start the car."

I said, "Well no, I want this to be automatic. I should be able to get in the car, turn the key and have the computer start too. The tape player in the car is for Bartok, not for Kansas City data." I paused slightly to allow the air to clear, and then continued. "I have been thinking of using nonvolatile programmable memory."

Ray's jaw dropped. "Nonvolatile? Do you mean *core* memory?"

While magnetic core memory is indeed nonvolatile, that was not what I meant. "No, not core, but *semiconductor, nonvolatile programmable memory!*"

Though Ray is quite technically aware, this was a new concept for him and he wasn't sure if I was serious. I have been known to play jokes like this before.

To convince him that I was serious, I began to explain, "Specifically, I am talking about *electrically alterable read-only memory*, or EAROM. You should consider it as a *read-mostly* memory."

"Well, that's different!" Ray exclaimed with relief. "You didn't say read mostly!"

All About the EAROM

EAROMs are *word-alterable* read-only memories intended for use as "read-mostly" memories. On the surface this may sound similar to an EPROM (erasable, programmable read-only memory). Once erased under ultraviolet light, an EPROM is indeed a word-alterable read-only memory.

In reality, there is very little similarity between the electrically alterable and erasable, programmable memory. An EPROM can be erased only in block mode and generally takes about 10 minutes to erase. While some can be programmed in as little as 50 seconds, an 11-minute (or more) read/write cycle-time hardly qualifies it in the category of high-speed programmable memory. An EPROM, therefore, is just a conveniently reprogrammable read-only memory.

An EAROM, on the other hand, does not rely upon ultraviolet light exposure for erasure. Clearing memory for reprogramming is done

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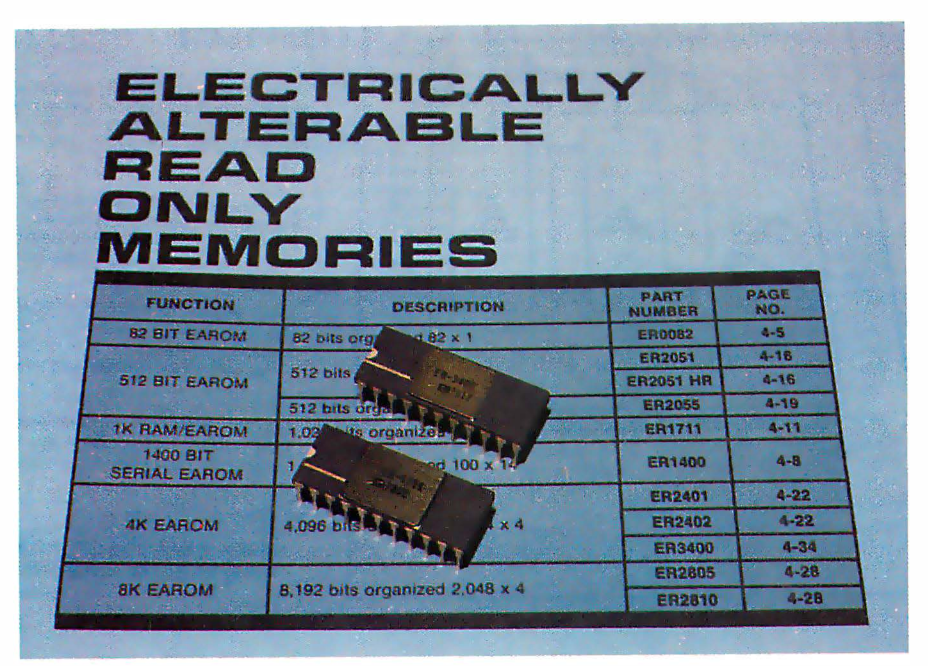


Photo 1: *Shown here are the General Instrument ER3400 and ER1711 electrically alterable read-only-memory (EAROM) parts. The ER3400 has only the EAROM function; the ER1711 combines the functions of programmable memory and EAROM in a single part.*

electrically. With a read time equivalent to a high-speed EPROM, complete or partial erasure in 10 ms, and a write time of a mere 1 ms, an EAROM fills the gap between truly programmable memory and EPROM.

EAROM can be integrated into the memory address space of practically any microcomputer. Like regular read-only memory, it retains data (for up to 10 years) when the power is removed, and is a natural choice for bootstrap program-storage applications. Should the stored program have to be changed, you can erase the chip with a 10-ms eraser routine and then rewrite the data at a rate of 1 ms per byte. This can all be done without removing the part from the system.

There are many EAROMs available, but like other types of memory devices, their architectures and capacities vary. You would not use 1 K-bit memory chips if you had to fit 64 K bytes of memory on a small printed-circuit board, nor would you choose to use an erasable programmable read-only memory requiring a 3-voltage power supply if only a 5-V supply is available.

It is important to observe that EAROMs also have limitations. Unlike regular programmable memory, the electrically alterable read-only memory cannot be erased and reprogrammed without limit. The General Instrument model ER3400 EAROM, for instance, can have each byte *read* 2×10^{11} times, but written only 100,000 times. If this EAROM were being used as standard programmable memory in a frequently executed loop, 100,000 erase and write cycles would take only 20 minutes.

The ER3400 is better used to store tables and calculated results that must be retained if the power fails. The specific, useful qualities of the ER3400 are high density of data storage, high speed, and long time of data retention.

A Hybrid Memory Device

Where nonvolatile memory is required to have more frequent write cycles, the General Instrument ER1711 should be used. This device combines two types of memory on a single chip: a standard 1 K-bit, static programmable memory and a 1 K-bit electrically alterable read-only memory.

Circle 225 on inquiry card.

A0 thru A9	10-bit word address.
D0 thru D3	Data input and output pins.
$\overline{CE}$	Chip enable. Chip selected when $\overline{CE}$ is pulsed to logic 0.
C0,C1	Mode-control inputs.
$\overline{WE}$	Write enable. Input data read when $\overline{WE}$ is pulsed to logic 0.
V_{SS}	Substrate supply. Normally at +5 V.
V_{GI}	Ground input.
V_{DD}	Power-supply input. Normally at -12 V.
V_{GG}	Power-supply input. Normally at -30 V.

Table 1: *Functions of pins on the General Instrument ER3400 electrically alterable read-only-memory device.*

The programmable memory is mapped as standard program memory. There is no limitation on write cycles. When the memory contents are to be retained, such as at the time of system power-down, a sensing circuit pulses the EAROM write line. With one pulse the entire content of the 1 K programmable memory is written in parallel to the EAROM. The EAROM section has the same write-cycle limitations as the ER3400 part.

Devices such as the ER1711 are particularly suited for storing frequently changing data. As long as power is available to the system, this data resides in the programmable memory. Only during periods when the power is off or during special events is the data transferred to nonvolatile storage.

Design Choices

Each of the two EAROM devices has its good and bad features. The designer choosing EAROM parts for a memory system will have to choose among the various positive attributes and complications. No single EAROM part necessarily fits all applications. The application must determine the choice.

Failure to understand this fact and lack of adequate knowledge of the variety of parts available are contributing factors to the absence of electrically alterable read-only memories in personal computers. The two devices I have chosen to discuss should cover most applications, but other configurations do exist.

General Instrument ER3400

The ER3400 is a 4 K-bit EAROM configured as 1024 by 4 bits. 1 K bytes of nonvolatile storage can be obtained using two chips. Figure 1a shows the pinout designations, and figure 1b shows the block diagram of the chip. Photo 1 shows the part in its dual-in-line package. Table 1 describes the functions of the pins found on the ER3400.

The ER3400 requires three power-supply voltages (+5 V, −12 V, and −30 V) for complete operation.

Because of the relatively low currents required to write data into an EAROM, the −30-V supply is usually derived from either the +5-V or −12-V supply. A previous Circuit Cellar article ("No Power for Your Interfaces? Build a 5 W DC-to-DC Converter," October 1978 BYTE, page 22, or page 1 in my book *Ciarcia's Circuit Cellar* BYTE Books, 1979) covered both theory and design procedures, should you need to make −30-V supply.

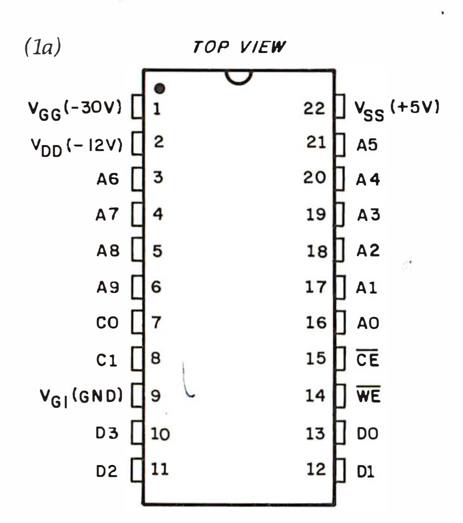
Unlike a regular programmable memory which has only read and write functions, the ER3400 has four operational modes: read; write; word erase; and block erase.

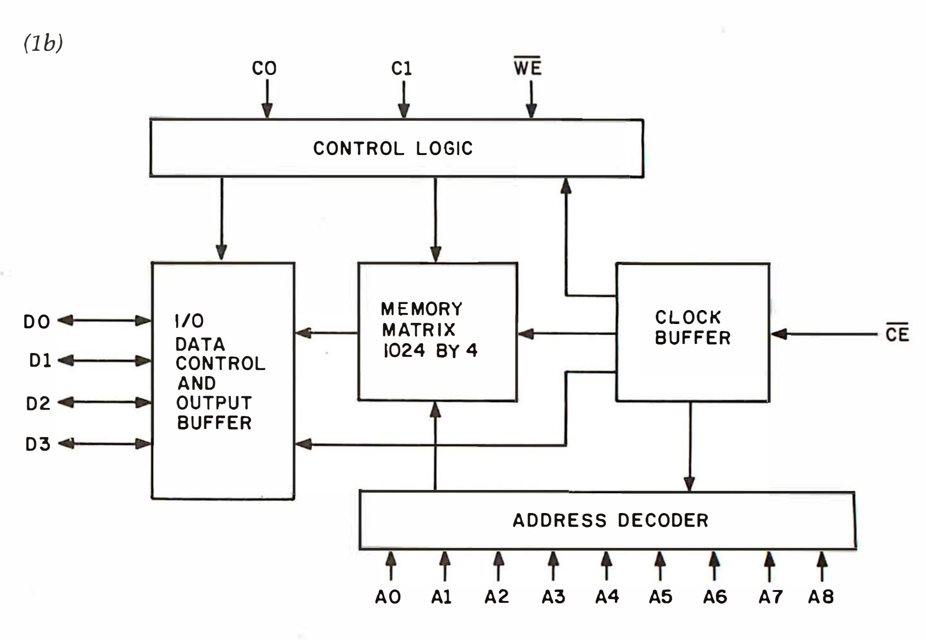
Operational Modes of the ER3400

Erase: To erase one word, both of the C0 and C1 mode-control input lines are set in the logic 1 (high) state, and the desired address location is set. A negative excursion of the voltage on the chip enable ($\overline{CE}$) line loads in the address and control, and initiates the erase operation. To avoid tying up the microprocessor bus, this mode is latched on the positive-going edge of the $\overline{CE}$ signal. The erase operation will continue while $\overline{CE}$ is high.

When it is desired to erase the entire device, the operation is the same,

Figure 1: *Pinout designations of the twenty-two pins on the General Instrument ER3400 electrically alterable read-only memory (1a), and a block diagram of the major circuit sections within the part (1b).*





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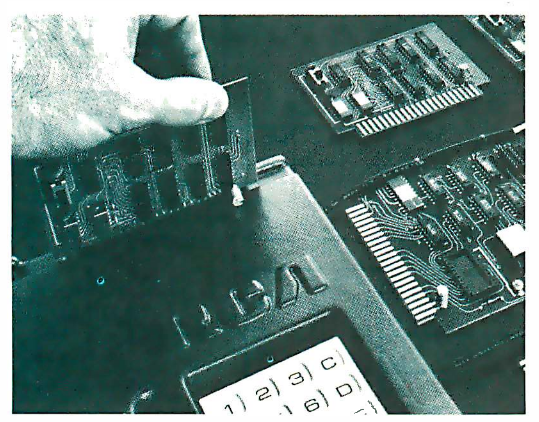
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C0	C1	Mode	Explanation
0	1	Block erase	Erase operation performed on all words.
1	1	Word erase	Stored data is erased at addressed location.
0	0	Read	Addresses data read after leading edge of CE pulse.
1	0	Write	Input data written at addressed location.

Table 2: *Selection of modes of operation of the ER3400 EAROM. The indicated logic levels are presented to the two mode-control inputs C0 and C1 to produce the corresponding mode of operation of the memory device.*

except that the C0 mode-control input is low while C1 is kept in a high logic state.

A "dummy read" operation is required to end the erase cycle.

Write: The control code for write is for the C0 line to be high while C1 is low. The control word and address are strobed in at the occurrence of the CE (chip enable) pulse. Data is strobbed in during the write enable (WE) signal. The timing requirements for the write enable signal are designed so that WE may be generated by combining the chip enable signal and a write signal through a logic gate.

As is the case with the erase operation, the control code and address are latched on the rising (positive-going) edge of CE. Data is latched by the rising edge of WE. As in erase, a dummy read is required to end the write cycle.

Read: To read out data, C0 and C1 control lines are both held low and the desired address is selected. The chip enable signal strobes in the mode and address data, and clocks out the data.

In all modes, when CE is high, the data input/output lines are in a high-impedance state. The control line logic levels for the several modes are summarized in table 2.

In the write and erase (both word and bulk) modes, the data, addresses, and the state of the control lines are loaded into internal registers within the ER3400 on the rising edge of the CE pulse, and are later cleared by a dummy read pulse also strobed by CE.

Number	Type	+5 V	GND	-12 V	-30 V
IC1	HM-7603	16	8		
IC2	ER3400	22	9	2	1
IC3	ER3400	22	9	2	1
IC4	74121	14	7		
IC5	7400	14	7		

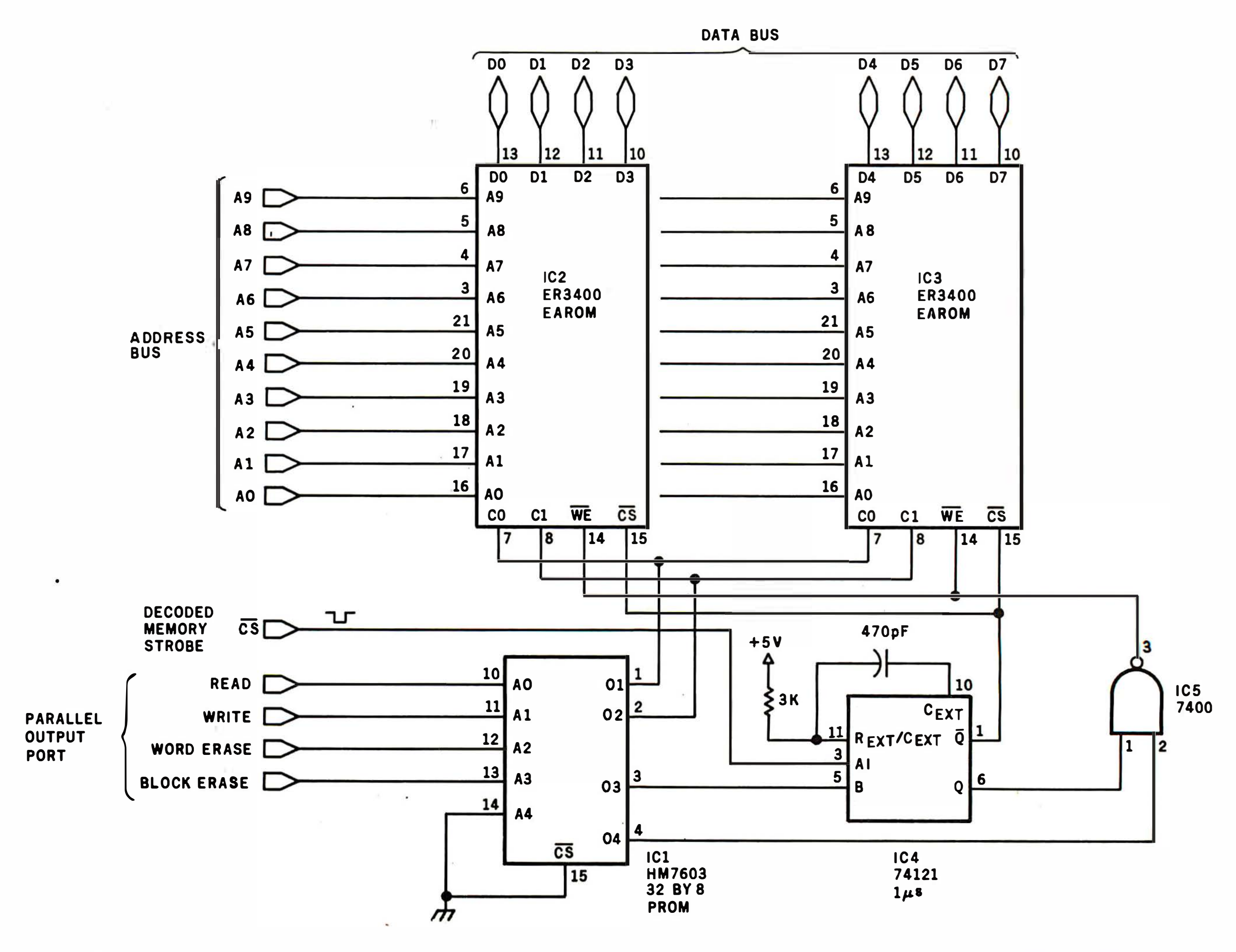


Figure 2: *Schematic diagram of a circuit that uses two ER3400s to form a 1024-byte memory. Read, write, and erase functions of the ER3400 are available using this circuit. The programmable read-only memory, IC1—the Harris Semiconductor HM-7603, a 32-word-by-8-bit PROM, serves to decode mode-control inputs received from a parallel output port. The truth table for this PROM is shown in table 3.*

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Operation	Address A0	A1	A2	A3	A4	Data O1	O2	O3	O4	O5	O6	O7	O8
Read	1	0	0	0	0	0	0	1	0	X	X	X	X
Write	0	1	0	0	0	1	0	1	1	X	X	X	X
Word Erase	0	0	1	0	0	1	1	1	0	X	X	X	X
Block Erase	0	0	0	1	0	0	1	1	0	X	X	X	X
All other locations						0	0	0	0	X	X	X	X

Table 3: *Truth table for the mode-decoding, programmable read-only memory (PROM) that appears as IC1 in figure 2. A high logic state is represented by 1; a low logic state is represented by 0. Where the logic state does not matter, X characters appear in the table. Possible substitutes for the Harris Semiconductor HM-7603 PROM used here include the 74S288, 82S123, and AM27S09.*

Observe carefully the requirement for the dummy read operation. Since there is no internal timing or sequencing, the ER3400 relies upon the user to terminate the write and erase functions by switching the EAROM into the read mode after 1 ms following a write and after 10 ms following an erase. There are various software and hardware methods to accomplish this.

For personal computer use, the circuit of figure 2 should be considered. A parallel output port provides the flag input to the mode-decoding, programmable read-only memory (PROM) IC1. A memory map of the mode-decoding memory is shown in table 3.

With the electrically alterable read-only-memory device attached to the address and data lines, a read operation is accomplished by setting the output bit corresponding to the A0 input line of the PROM to a high logic state. Each of the four address lines A0 thru A3 is called a flag for purposes of explanation.

Setting the read flag (A0) corresponds to a binary 10000 input code to the PROM (IC1 in figure 2). The O1 and O2 outputs will place low logic levels on both mode-control inputs C0 and C1. This places the EAROM in the read mode.

Next, the EAROM is addressed through the normal $\overline{CS}$ line. This action fires the one-shot (monostable multivibrator, IC4 in figure 2) which clocks the data onto the computer data bus. The ER3400 has a cycle time of 1.8 μs. Depending upon the memory speed of your computer, it may be necessary to add wait states when addressing EAROM.

The sequence is similar for write and erase operations. By setting the write flag (A1), the mode-decoding PROM causes C0 to go high while C1 stays low, placing the EAROM in the write mode. Addressing the appropriate byte and strobing the $\overline{CS}$ line causes the ER3400 to enter a write

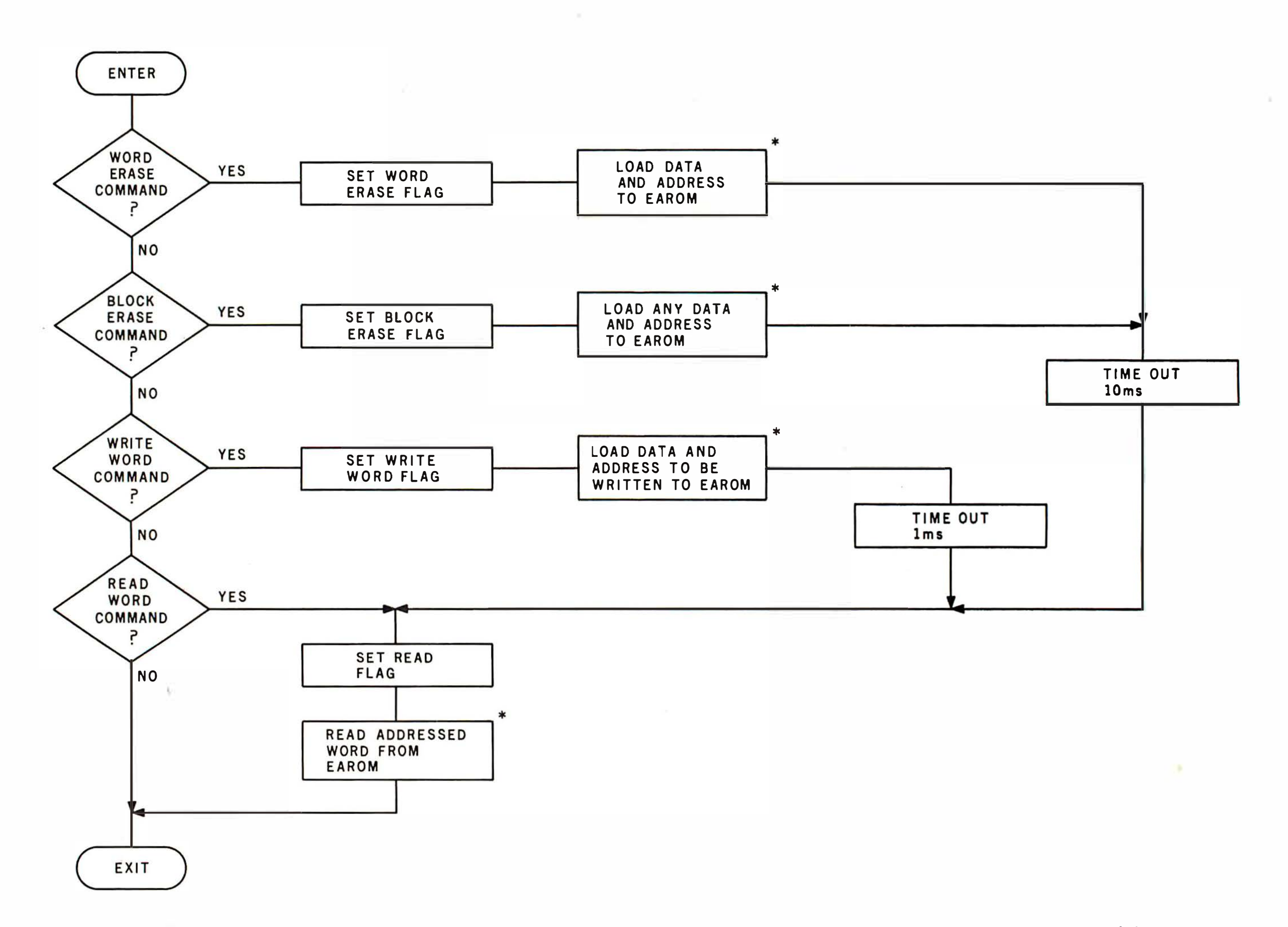


Figure 3: *A flowchart of the algorithm for actuating the various operating modes of the ER3400 interface circuit of figure 2. The diagram blocks marked with asterisks refer to standard memory read or write instructions.*

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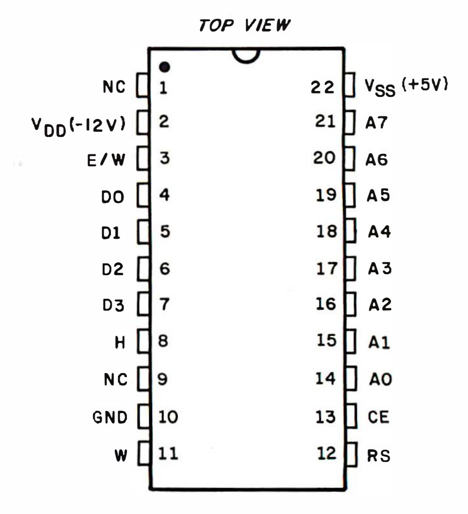
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Table 4: *Descriptions of pin functions of the General Instrument ER1711 hybrid EAROM/programmable memory part.*

Pin	Description
D0 thru D3	4-bit data word
A0 thru A7	8-bit data address
V_{SS}	+5-V supply voltage
V_{DD}	−12-V supply voltage
V_{GI}	Ground
CE	Chip enable: strobed during programmable-memory cycles, held low during EAROM cycles
H	Hold: normally high, low during data-recall cycle
W	Write: high during programmable-memory write cycle
RS	Restore: normally low, pulsed high during recall cycle
E/W	Erase/Write: controls EAROM memory cells.

Figure 4: *Pinout designations of the General Instrument ER1711 hybrid electrically alterable read-only-memory/programmable-memory device.*



condition. (The byte addressed for writing should have previously been erased through either the word or block erase operations.)

After 1 ms, the read flag (A0) is set and a read sequence is executed to stop the write activity. A flowchart of the mode-selection algorithm is shown in figure 3.

Operational Modes of the ER1711

The ER1711 operates quite differently from the ER3400. Configured as 256 by 4 bits, this device combines the properties of both regular programmable memory and electrically alterable read-only memory on a single chip. Figure 4 shows the pinouts of the ER1711, and table 4 describes the pin functions.

In general, EAROM writing is rather slow. Read access time can be less than 1 ms, but writing and erasing take 1 to 50 ms (depending upon the device). As demonstrated earlier, it takes a little over 1 second to completely write the ER3400.

In applications where the EAROM is "read-mostly" memory and is used to hold infrequently changing data or programs, slow erase and write times are no problem. However, in instances where an EAROM is used to store data or programs during power-down conditions, slow write times are objectionable. The distinctive feature of the ER1711 is its ability to store its entire contents of the programmable memory in a single write pulse.

The static programmable-memory section of the ER1711 is addressed like any other system memory. It can hold constantly changing data with no restrictions on the number of read/write cycles. The contents of this memory can be transferred to the EAROM section through one write pulse. In this way, the EAROM can instantly save all data when the power fails. When power is returned, a simple pulse sequence restores the data from the EAROM to the programmable operating memory.

ER1711 Power Requirements

The ER1711 uses +5-V and −12-V power supplies for normal programmable-memory operation. These supplies must be kept constant within a 5% tolerance. Other voltages used are as follows for EAROM operations:

V_W (−17 V to −21 V)

is used to transfer data from programmable memory to EAROM;

V_R(−8 V to −15 V)

is used to transfer data from EAROM to programmable memory; and

V_E (+25 V to +30 V)

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is used for erasing the EAROM storage cells.

Since these voltages are required only as single pulses during either power-up or power-down cycles, they do not require separate power supplies. All voltages can be generated by charge-pumping circuits operated from +5-V and −12-V supplies.

Figure 5 is the schematic diagram of a circuit which accomplishes the save-data and recall-data functions and maintains the proper timing and voltages required for the various operations.

Data Restoration

The static-programmable-memory portion of the ER1711 has an access time of 900 ns. Upon initial application of power to the system, if this programmable memory is to be loaded from EAROM, the computer signals this action by pulsing the *data-recall* input line. This triggers a 300 μs ramped voltage to the erase/write (E/W) line of the ER1711. After 300 μs, the hold line (H) is brought high for 150 ms, and the E/W line is set at a potential of 27 V. At the conclusion of this sequence, the ER1711's programmable memory will contain the former contents of the EAROM, and the EAROM will be erased.

Saving the data stored in the programmable memory is started by raising the *system-save* line to a logic 1. The resultant application of a −20-V pulse of a 1-to-10-ms duration to the ER1711 causes the data to be stored in the electrically alterable read-only memory. Data retention time varies according to the pulse duration, from 3 days for a 1-ms pulse to 30 days for a 10-ms pulse.

In Conclusion

I do not expect that you will immediately convert your computer memory to EAROM, but at least you now know what EAROM is. In my own case, I have chosen to use ER1711 memory devices for my automotive computer. I can only speculate on the final configuration, but at least I can count on not having to be concerned with standby power consumption and battery backup.

Figure 5: *A circuit that allows data stored in the programmable memory of the ER1711 to be saved into and recalled from the electrically alterable read-only-memory section. Charge-pumping circuits are used to generate the relatively high voltages needed for the erase, store, and recall cycles of the ER1711. Power-down and power-up states are initiated by the System Save and Data Recall signals.* →

For further information on EAROMs or determination of price and availability contact:

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EAROM specifications and diagrams reprinted courtesy of General Instrument Corporation.

Next Month: you will learn how to build a wireless interface that connects the Sears (alias BSR) home control system to your computer. ■

Operation of the ER1711

In normal operation the ER1711 operates as a programmable memory. Before powering down, the data can be stored in the electrically alterable, nonvolatile read-only-memory (EAROM) cells by a single, negative write pulse. When power is restored, the previously saved data can be recalled by a power-up and data-recall cycle which transfers all this saved data to the programmable memory. It is suggested that an erase cycle be performed soon after the data-recall cycle, so that the memory will be prepared in case of another power-down cycle. The EAROM cycles operate as explained here.

Erase Cycle:

1. *The H line should be high and the RS and CE lines low.*
2. *Positively pulse the E/W line to +25 V for 100 to 200 ms.*

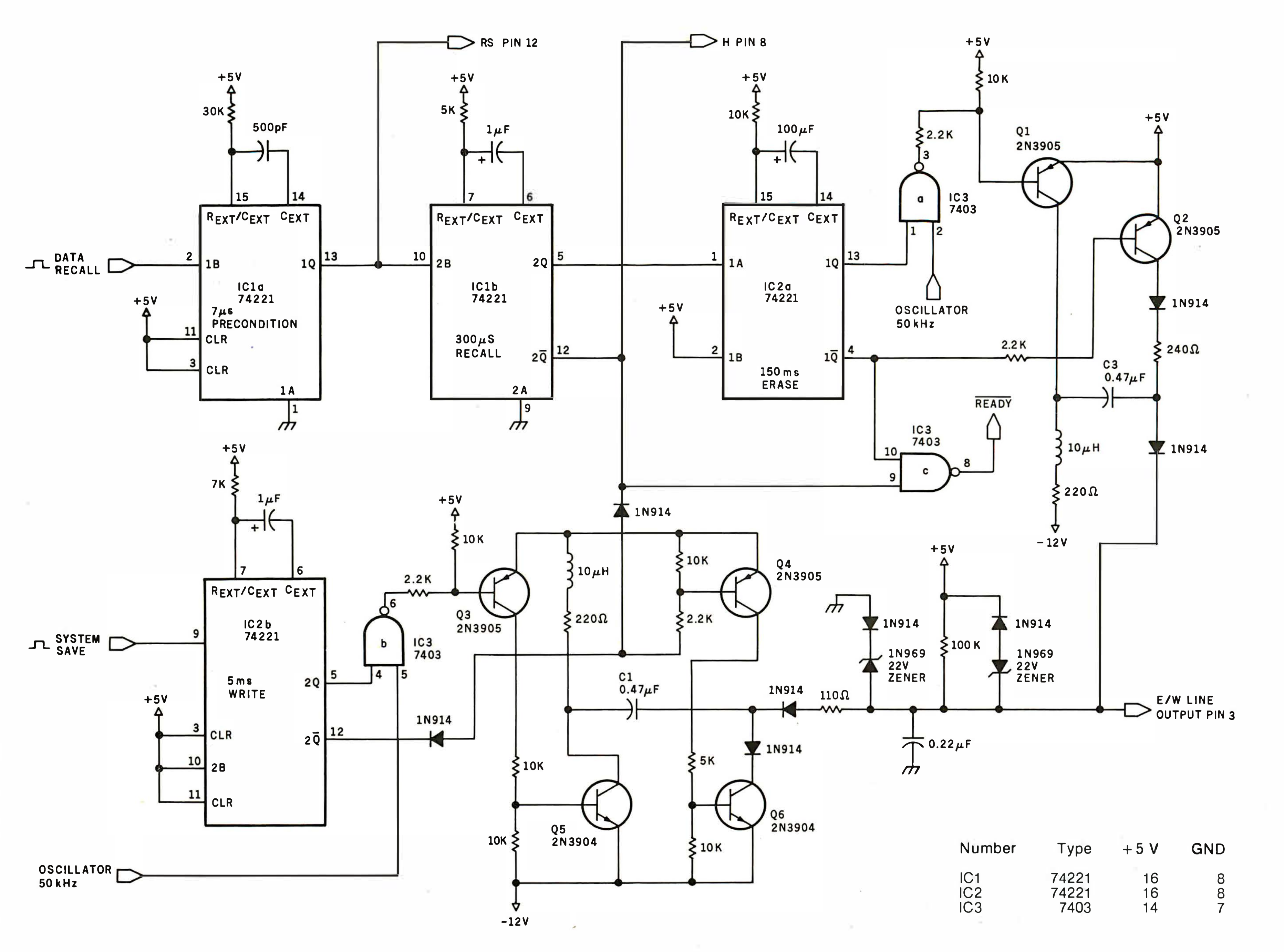
Stored-Data Cycle:

1. *The H line should be held high and the RS and CE lines low.*
2. *Pulse the E/W line negative to -22 V for 1 to 10 ms to store nonvolatile data.*
3. *The nonvolatile EAROM memory cells must have been previously erased for valid data retention.*

Power-Up and Recall Cycle:

1. *Turn on power with CE and RS held to ground and the H and E/W lines based to V_{ss}.*
2. *When power is on, lower H and pulse RS to precondition the EAROM cells.*
3. *Lower RS and ramp down the E/W line at a rate of -0.1 V/μs. This can be done with a series resistor of 470 K ohms in the E/W line.*
4. *After the E/W recovery time, bring both the E/W and H lines to $+V_{ss}$.*
5. *If in the course of erasing data, the power shuts down again, the erase cycle can be terminated and a write cycle immediately started without loss of data.*

In normal programmable-memory operation, only the +5-V and -12-V power supplies are required. The erase-store and recall cycles require momentary high-voltage pulses to tunnel charges through the negative-metallic-oxide-semiconductor (NMOS) memory transistors. These higher voltages can be created from the +5-V and -12-V power supplies using the charge-pumping circuits shown in figure 5. This circuit will generate the sequence of RS, H and E/W pulses needed for power-down and up sequencing. The power-down and up cycles are initiated by System Save and Data Recall signals respectively. Figure 5 is a suggested circuit using standard transistor-transistor logic (TTL) parts; a similar circuit can be designed with complementary-metallic-oxide-semiconductor (CMOS) logic instead.



Number	Type	+5 V	GND
IC1	74221	16	8
IC2	74221	16	8
IC3	7403	14	7

Faster Audio Processing with a Microprocessor

William J Dally
Apt U-3 Dutch Village
Blacksburg VA 24060

Introduction

Audio processing involves transforming an audio signal by filtering, delay, and modulation to make the sounds more musically pleasing or to improve communication systems. Audio processing by both analog and digital methods has been performed for many years; however, these methods are expensive to implement if complete manipulation of the ouput signal is to be achieved.

The advent of low-cost microcomputers in recent years permits a new approach to audio processor design which has the advantage of much greater flexibility at competitive costs. T C O'Haver employed a microcomputer for audio processing using a minimum of hardware in the design, while relying upon software for signal manipulation (see "Audio Processing with a Microcomputer," June 1978 BYTE, pages 166 thru 173). With this heavy emphasis on software, the speed of the processor was not sufficient to process high fidelity audio signals (20 Hz to 20 kHz). This article presents a different approach wherein modest amounts of hardware are incorporated into the design of the microcomputer system, reducing the demands on the processor. Flexibility in manipulating the audio signal is not sacrificed, and the cost of the additional hardware is not excessive.

About the Author

William J Dally is an engineering consultant for a Silver Spring, Maryland electronics development firm and is an electrical engineering student at Virginia Polytechnic Institute and State University. His past projects include a programmable read-only memory programmer, a computerized traffic control system, and an intelligent tape drive; current projects include a general purpose Z80 system and a disk-based editor plus assembler which uses only 3 K bytes of memory.

Timing Analysis of Software Approach

In the microcomputer audio processing system developed by O'Haver, only an analog-to-digital (A/D) converter, a microprocessor, and a digital-to-analog (D/A) converter were used. The audio processing functions of phlanging, reverberation, and linear transformation were performed by the software of the system. In a timing analysis of the design, an 8080 processor operating at a system clock rate of 2 MHz was considered.

The processing routines used in this system are shown in listing 1, translated to 8080 assembly language. Also shown are the number of processor cycles and the execution times for these routines (28 μs, 79 μs, and 85 μs respectively). Most applications will use all three of these routines, as well as system control and overhead routines. Thus, the worst-case cycle time (the time required to process one unit of data) becomes:

$$t_{cy} = 28+79+85+t_{ov} > 200\ \mu s$$

where t_{cy} = worst-case cycle time and t_{ov} = overhead time.

To prevent distortion, the sampling frequency f_n must be twice that of the maximum signal frequency f_s which is:

$$f_s < f_n/2 = 1/(2t_{cy}) < 2.5\ \text{kHz}.$$

It is evident from this calculation that $f_s <$ 2.5 kHz is too low for high-fidelity audio. Furthermore, many audio applications require more functions than linear transformation, phlanging, and reverberation. Adding more functions to a software-oriented system decreases the maximum signal frequency still further. It is apparent that a system which depends too heavily on software is too slow for comprehensive audio processing. A better approach is to use a design combining software and hardware that reduces the time demands on the processor, while maintaining flexibility.

Hardware and Software Approach

There are several methods by which hardware can be added to the system to reduce the processing load. Bit-slice processors with cycle times which are about eight times faster than an 8080 could be used for the processor. However, these bit-slice processors and the fast memories needed to support them are prohibitively expensive. Also, this system would not be capable of handling any additional functions.

A better solution is to add peripheral hardware to take some of the processing load off of the pro-

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```
;           XFER    — ROUTINE FOR LINEAR TRANSFORMATIONS                    (CLOCK CYCLES)
XFER:       LHLD    CONV          ;GET INPUT FROM ADC                           16
            STA     STRB          ;STROBE ADC                                   13
            MVI     H,TABLE       ;POINT AT TABLE                                7
            MOV     A,M           ;GET TRANSFORMED DATA                          7
            STA     DAC           ; OUTPUT TO DAC                              +13
;EXECUTION TIME 28 MICROSECONDS                                                 56
;
;           PLNG    — PHLANGING ROUTINE
PLNG:       LHLD    DELAY         ;GET STARTING DELAY                           16
NEXT:       MVI     H,BUFF        ;POINT AT BUFFER                              13
            MOV     A,M           ;GET DELAYED DATA                              7
            ANI     FEH           ;DIVIDE BY TWO                                 7
            RRC                   ;                                              4
            MOV     B,A           ;SAVE FOR MIXING                               5
            LDA     CONV          ;GET NEW DATA                                 13
            STA     STRB          ;STROBE ADC                                   13
            MOV     M,A           ;PUT IN CURRENT BUFFER LOCATION                7
            ANI     FEH           ;DIVIDE BY TWO                                 7
            RRC                   ;                                              4
            ADD     B             ;MIX NEW AND DELAYED SIGNALS                   4
            STA     DAC           ;OUTPUT TO DAC                                13
            DCR     L             ;NEXT LOCATION                                 5
            JNZ     NEXT          ;NOT DONE — NEXT LOCATION                     10
            LXI     H,DELAY       ;DONE — SWEEP DELAY                           10
            DCR     M             ;                                             10
            JMP     PLNG          ;REPEAT                                      +10
;EXECUTION TIME 79 MICROSECONDS                                                158
;
;           RVRB    — REVERB ROUTINE
RVRB:       XRA     A             ;INITIALIZE BUFFER ADDRESS                     4
            MOV     L,A           ;                                              5
            MOV     H,A           ;                                              5
RRST:       MVI     H,FIRST       ;POINT AT BEGINNING OF BUFFER                 13
RNXT:       STA     STRB          ;STROBE ADC                                   13
            MOV     A,M           ;GET DATA FROM BUFFER                          7
            ANI     FEH           ;DIVIDE BY TWO                                 7
            RRC                   ;                                              5
            MOV     B,A           ;SAVE FOR MIXING                               5
            LDA     CONV          ;GET DATA FROM ADC                            13
            ANI     FEH           ;DIVIDE BY TWO                                 7
            RRC                   ;                                              5
            ADD     B             ;MIX                                           4
            MOV     M,A           ;STORE MIXED SIGNAL IN BUFFER                  7
            STA     DAC           ;OUTPUT TO DAC                                13
            INR     L             ;INCREMENT POINTER                             5
            JNZ     RNXT          ;NOT DONE — GO REVERB                         10
            INR     H             ;MAYBE DONE, CHECK H                           5
            LDA     LAST          ;                                             13
            CMP     H             ;                                              4
            JZ      RRST          ;DONE — START BUFFER OVER                     10
            JMP     RNXT          ;NOT DONE                                    +10
;EXECUTION TIME 85 MICROSECONDS                                                170
```

Listing 1: *Audio processing routines to perform linear transformation, phlanging, and reverberation, using a software-oriented approach on an 8080 system with a 2 MHz system clock frequency. Execution times of 28 µs (linear transformation), 79 µs (phlanging) and 85 µs (reverberation) are too slow for high-fidelity audio applications.*

cessor. This distributed hardware approach is less expensive than a fast processor, and allows more flexible software since timing is not critical. The remainder of this article will discuss this approach.

System Definition

To design an audio processing microcomputer system, it is necessary to define the system's processing functions. These functions fall into three categories: linear transformations, time-delay functions, and gain-control functions. Functions such as distortion and clipping, where the output depends only on the input, are linear transformation. Time-delay functions such as phlanging, phase shifting, and reverberation, involve delaying the incoming signal and mixing signals which are delayed for different amounts of time. Gain-control functions involve varying the gain of the system to control amplitude, and include sustain, vibrato, and quantization noise reduction.

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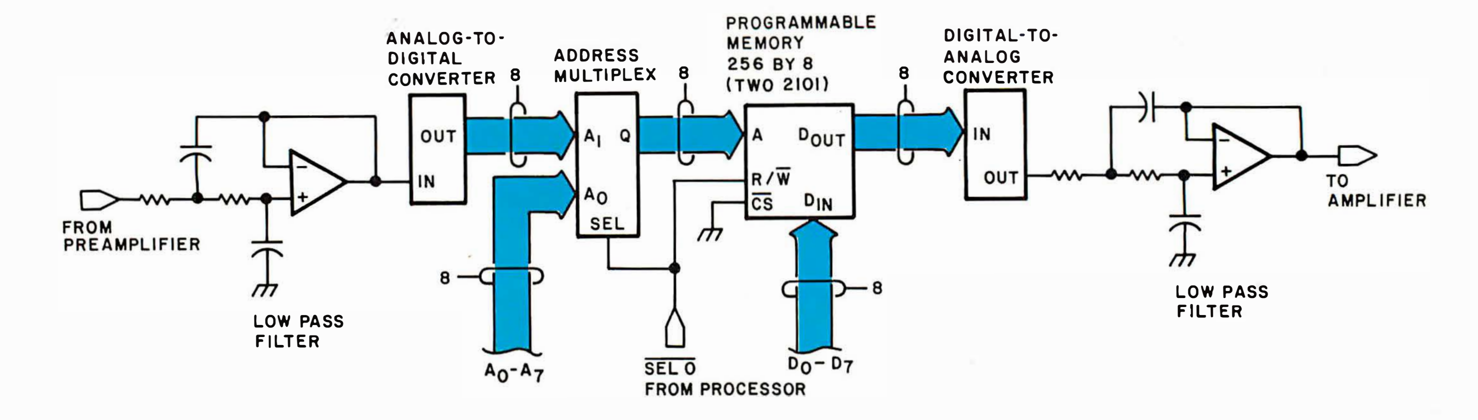


Figure 1: *A simplified diagram of a hardware implementation of a linear transformation or transfer function. It requires a software routine to set up a transfer function in a look-up table stored in memory.*

Linear Transformations

A simplified diagram of a hardware implementation of a linear transformation is shown in figure 1. In this system, the audio input is filtered to eliminate high-frequency noise, and converted to digital form. This digital signal is then used as the address for a look-up table stored in memory. An address multiplexer allows the processor access to the memory to set up or change the table. The output of this table is converted to analog form and is filtered to limit it to audio frequencies. Thus, the ouput is an audio signal, the voltage of which forms a one-to-one correspondence with the input voltage.

The only software required to support this hardware is a routine to set up a transfer function in the look-up table. This routine is executed only on power-up or when the transfer function is changed. Effects such as "fuzz," and harmonic distortion can be implemented in this manner, and users can define their own transfer function. A linear transfer function can be used to bypass this processing element if desired.

Compared to a software intensive approach, the only additional hardware required to implement a linear transformation is the address multiplexer. The converters and memory for a look-up table are required even with a software-oriented approach. However, the processor has much more free processing time with a hardware and software approach since data transfer takes place without processor intervention.



Time-Delay Functions

Phlanging is a time-delay function which involves delaying the input signal from 0 to 5 ms and mixing it with the current input signal to produce the output signal. The result is that of a comb filter, attenuating the frequency which has a period twice as long as the time delay and all of its odd harmonics. The time delay is varied with time over a certain range to give a sweeping effect.

Because a musician does not always want the same phlanging effect, it is necessary to give the processor control over the phlanging parameters, which include width (the difference between the longest and shortest time delay), range (the average delay), rate (the rate at which the delay changes), and depth (the amplitude of the delayed signal).

The hardware to perform the phlanging function is shown as a

Figure 2: *A diagram of hardware to perform the phlanging function. Phlanging is an audio effect originally produced by playing duplicate tape or disk recordings in almost exact synchronization. The name is derived from the practice of manipulating the phlanges of tape reels as they spin to change the degree of synchronization.*

simplified diagram in figure 2. The input signal is filtered, converted to digital form, and stored in memory for a period of time controlled by the processor. After being delayed by storage in memory, the data is converted to analog form (with the gain controlled by the processor), then mixed with the current incoming signal, and filtered. The mixing of a delayed signal with a signal which has not been delayed produces the phlanging effect.

The delay in memory is accomplished by having a counter cycle through a portion of the memory, reading the delayed data and writing new data at each location. Thus, the delay is equal to the cycle length which is controlled by the processor. The processor stores the cycle length in an 8-bit latch. The contents of this latch are compared to the output of the counter; when they are equal, the counter is reset to zero. This action causes the memory to cycle from location zero to the location corresponding to the contents of the latch. Thus, the processor can add sweep to the phlanging effect, and control the width, range, and speed of the sweep by varying the contents

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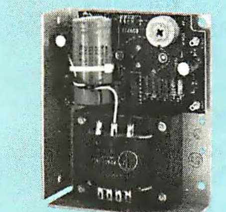
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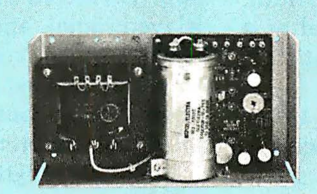
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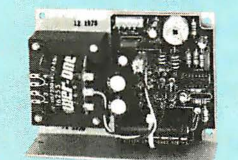
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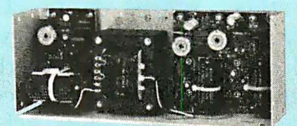
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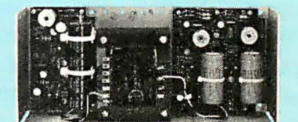
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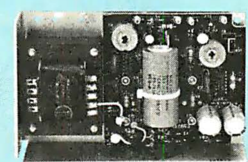
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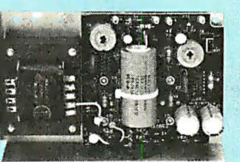
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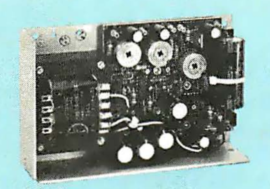


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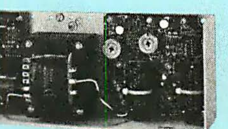
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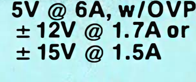
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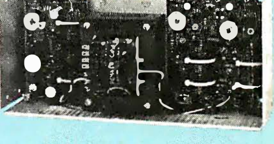


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of the 8-bit latch. The amplitude of the output is controlled by varying the reference voltage for the digital-to-analog converter.

A flowchart of a routine which will control the phlanging effect is shown in figure 3, and the 8080 code is shown in listing 2. This routine should be supported by a control panel routine which updates the values of amplitude, width, range, and speed from external switches.

The routine initially sets the time delay equal to range plus ½ width. This delay is then decremented at a rate proportional to speed until the delay becomes equal to the lower limit of range minus ½ width. When this value is reached, the process is repeated with the delay being set to its initial value.

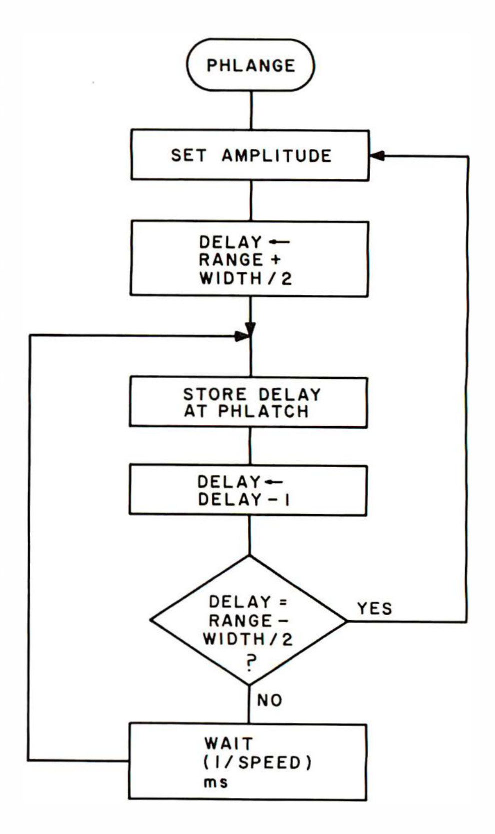
For this routine to operate efficiently, the wait period of (1/speed) is regulated by a real-time clock interrupt. No processing time is wasted in software timing loops using this method. Allowing a minimum wait-time of 1 ms, this software will execute during 43 μs (average) out of every 1 ms interval. Comparing this value to the impractical execution times for a software-oriented approach, it is apparent that the addition of a little hardware takes a great load off the system software.

Reverberation (or reverb), another time-delay function, has the effect of making music sound like it is being played in a large auditorium. This effect is produced by creating artificial echoes, using time delay, that simulate echoes off the walls of a concert hall. Multiple echoes, from repeated reflections off walls, are simulated by mixing the ouput (delayed signal) with the input (not delayed) so that the output contains information that is delayed many times. To simulate different room acoustics, it is useful for the processor to have control over the length of the delay and the amplitude of the delayed signal.

A simplified diagram of a hardware implementation of the reverberation effect is shown in figure 4. The audio input is filtered and mixed with the delayed signal, and the output of this mixer is then converted to digital form and delayed in memory using a scheme analogous to that used in phlanging, with the processor controlling the length of the delay to simulate larger or smaller rooms. The output of the delay memory is converted back to analog form, with the amplitude controlled by the processor to determine the rate at which the echoes decay. This delayed analog signal is mixed with the input, producing the reverberation effect. The output is the current input signal *mixed* with echoes of an integer number of time periods with decaying amplitude.

At first the circuit described by figure 4 may appear to represent more than a little additional hardware. However, the 4 K bytes of delay memory are required even with an all software approach. Furthermore, the hardware reverberation circuit provides automatic refresh for dynamic memories, as the low-order six address bits are always cycled through

Figure 3: *Flowchart of software routine to control phlanging. The code for this routine is found in listing 2. It initializes the delay time to (range + width/2) and decrements the time at a rate proportional to speed until the delay time is equal to (range − width/2). When this value is reached, the delay time is reinitialized and the process is repeated. The average execution time is 43 μs for each cycle.*




```
                                                              (CLOCK CYCLES)

PHLN1:   LDA   AMPL    ;INITIALIZE — SET AMPLITUDE                 13
         STA   DAC3    ;ANALOG CHANNEL 3                           13
         LDA   STDEL   ;(RANGE + WIDTH/2)                          13
         STA   DELAY   ;DELAY ← RANGE + WIDTH/2                    13
         RET           ;                                           10
;
PHLNG:   LDA   DELAY   ;GET DELAY                                  13
         STA   PHLTC   ;STORE AT PHLATCH                           13
         DCR   A       ;DECREMENT DELAY                             5
         STA   DELAY   ;SAVE                                       13
         MOV   B,A     ;                                            5
         LDA   ENDEL   ;(RANGE − WIDTH/2)                          13
         CMP   B       ;DELAY = RANGE − WIDTH/2?                    4
         JZ    PHLN1   ;YES, REINITIALIZE                          10
         RET           ;NO, RETURN FOR 1 MS WAIT                  +10
;EXECUTION TIME 43 MICROSECONDS AVERAGE                            86   AVG
```

Listing 2: *Assembler coding of a routine to control phlanging for the 8080 microprocessor. A flowchart of this is shown in figure 3.*

Figure 4: *Simplified diagram of a hardware implementation of the reverberation effect. This circuit produces artificial echoes using a time delay.*

every 1.28 ms. Thus, the circuit described by figure 4 represents a small amount of additional hardware since the dedicated 4 K memory is less expensive than adding 4 K bytes of memory to the processor unit.

The software to operate this circuit (flowchart shown in figure 5, code shown in listing 3) consists of a routine to update the length of the delay and the amplitude of the delayed signal every time the control panel routine is accessed. Again, by dedicating 4 K bytes of memory to reverberation and adding a little additional hardware, great software savings are realized.

Gain-Control Functions

The third class of audio processing functions to be discussed is gain-control functions such as compression and vibrato. *Compression* involves decreasing the system's gain as the amplitude of the input signal increases, and increasing the gain as the amplitude of the input decays, to keep the output at a near constant

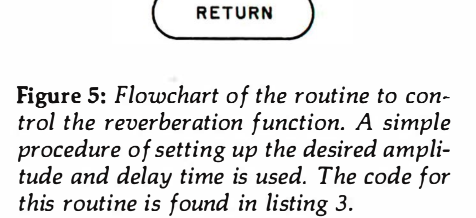
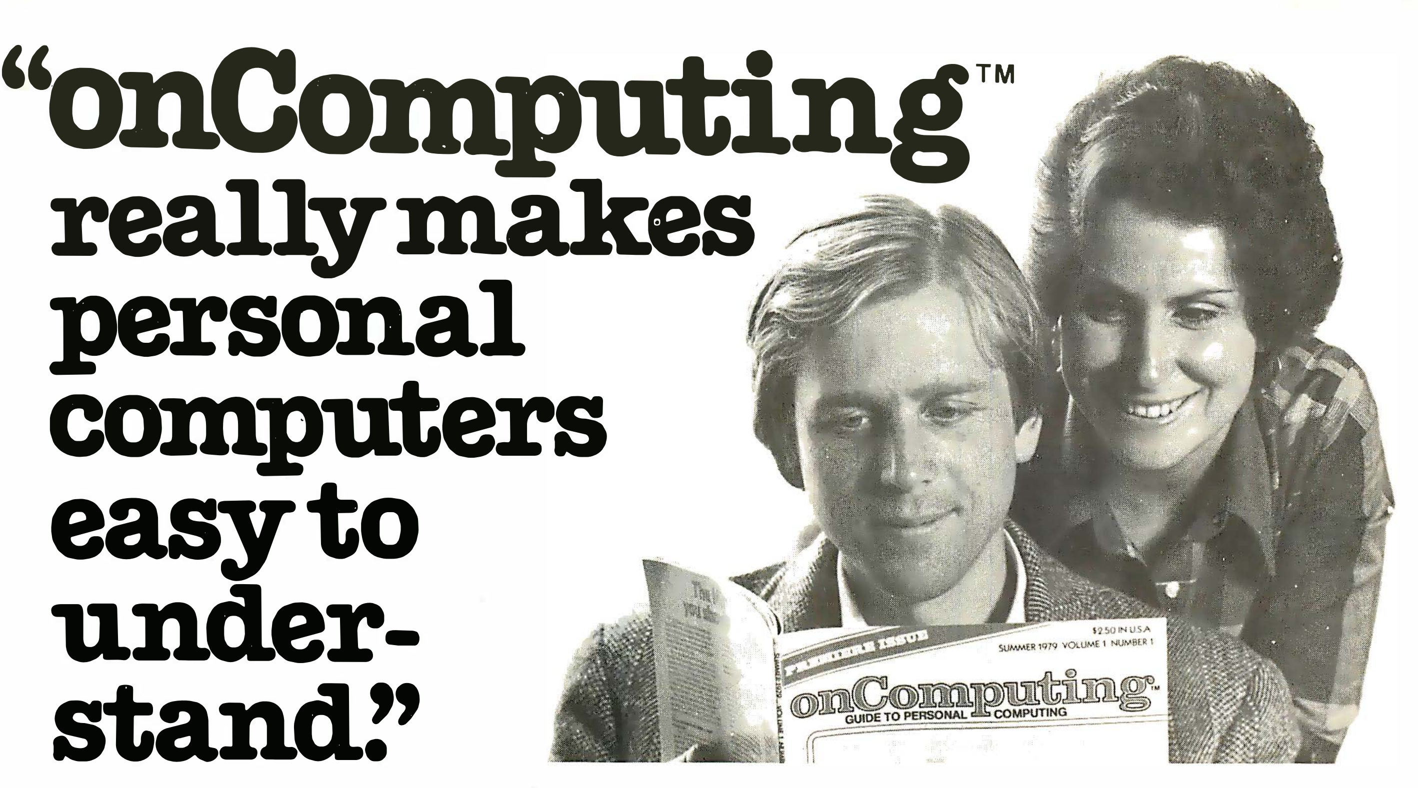


Figure 5: *Flowchart of the routine to control the reverberation function. A simple procedure of setting up the desired amplitude and delay time is used. The code for this routine is found in listing 3.*

```
                                                                (CLOCK CYCLES)
;REVB      — ROUTINE CALLED BY CONTROL PANEL TO SET UP REVERB
REVB:      LDA    RAMP        ;SET UP AMPLITUDE                      13
           STA    DAC2        ;ANALOG CHANNEL 2                      13
           LDA    RDEL        ;SET UP DELAY TIME                     13
           STA    RLTC        ;IN REVERB LATCH                       13
           RET                ;EXIT                                 +10
;EXECUTION TIME 31 MICROSECONDS                                      62
```

Listing 3: *8080 code of the routine to control the reverberation function. It simply sets up the desired amplitude and delay times. The flowchart is shown in figure 5.*



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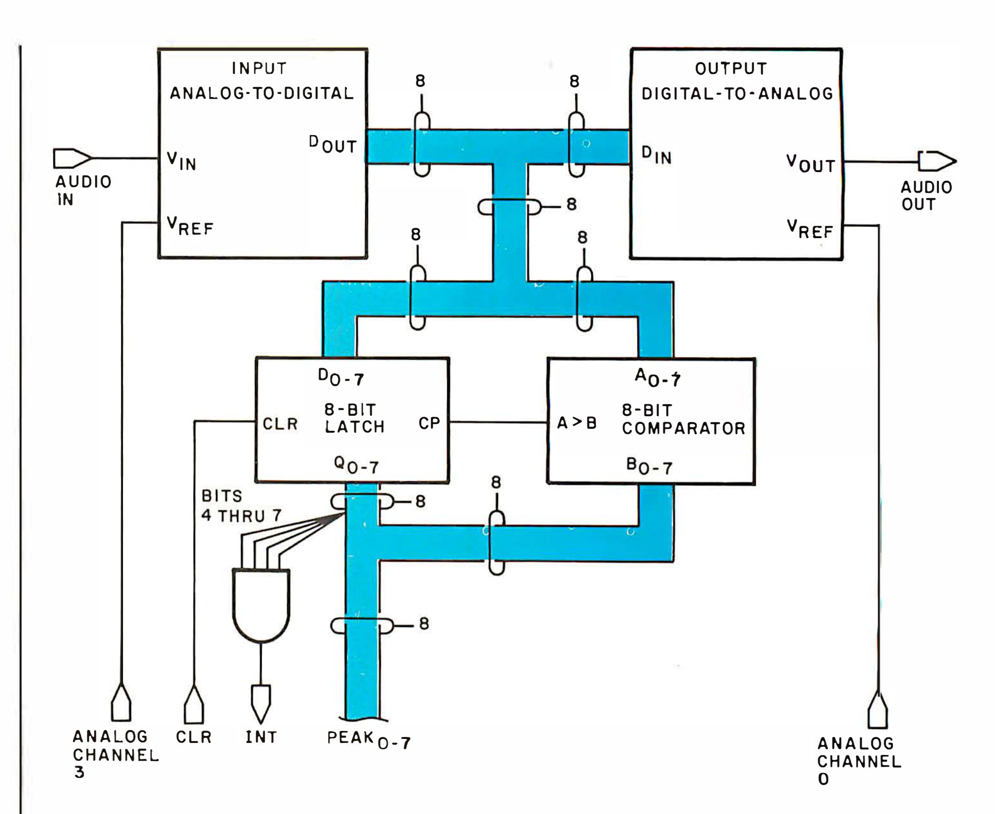


Figure 6: *Simplified diagram of a gain-control function circuit. It employs a feedback system using a digital peak comparator composed of an 8-bit latch and an 8-bit comparator.*

level. This effect "stretches" notes or sustains them by stopping their decay. *Vibrato* is an effect whereby the amplitude of the output is periodically varied to give a warbling sound.

The gain-control functions are implemented by means of a feedback system. The processor varies the gain of the system according to a certain rule and receives feedback on the result of its action by measuring the amplitude of the current signal. A circuit to perform these functions is shown in figure 6. The processor controls the amplitude of the signal by varying the reference voltages to the input analog-to-digital converter and output digital-to-analog converter. The processor gets feedback about the amplitude of the signal from a *digital peak detector* composed of an 8-bit latch and an 8-bit comparator.

To use the peak detector, the processor clears the latch at the beginning of a period and samples the contents of the latch at the end of the period. The comparator continuously compares the amplitude of the input signal (A) with the contents of the latch (B). When the amplitude of the incoming signal exceeds the value stored in the latch, the A>B output of the comparator goes to a *true* logic state, strobing the amplitude of the incoming signal into the latch. Therefore the contents of the latch always reflect the greatest amplitude of the input signal from the point when the latch was last cleared, because when a signal of greater amplitude is detected by the comparator, it is clocked into the latch.

Since the attack (rising amplitude portion of waveform) of the signal may be very fast, an interrupt is provided for the processor when the amplitude exceeds hexadecimal F0. This gives the processor time to adjust gain before clipping can occur.

A flowchart and code for the compression routine are shown in figure 7 and listing 4. This compression routine attempts to keep amplitude at a constant level by subtracting the peak value of the incoming signal from a limit on this value, set by the user. The reference voltage of the input analog-to-digital converter is adjusted proportionally to the difference. Thus, if the peak amplitude is lower than the desired limit, the difference is positive, and the analog-to-digital converter reference voltage (and therefore the gain) is increased. Similarly, if the peak amplitude is greater than the limit, the gain is

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```
;           COMPR  — PERFORMS COMPRESSION                      (CLOCK CYCLES)
COMPR:      LDA    LIMIT            ;GET LIMIT                        13
            MOV    B,A              ;SAVE                              5
            LDA    PKDET            ;GET PEAK                         13
            STA    CLRDET           ;RESET DETECTOR                   13
            SUB    B                ;PEAK — LIMIT                      4
            MOV    B,A              ;                                  5
            LDA    DAC3IM           ;GET CURRENT VALUE OF DAC3        13
            SUB    B                ;DAC3 + LIMIT — PEAK               4
            STA    DAC3IM           ;UPDATE DAC3 AND IMAGE            13
            STA    DAC3             ;                                 13
            RET                     ;EXIT                            +10
;EXECUTION TIME 53 MICROSECONDS                                      106
```

Listing 4: *8080 assembler code of the routine to perform compression of an audio signal by adjusting the reference voltage of the input analog-to-digital converter (ADC) to keep the output signal at a constant level. The flowchart is given in figure 7.*

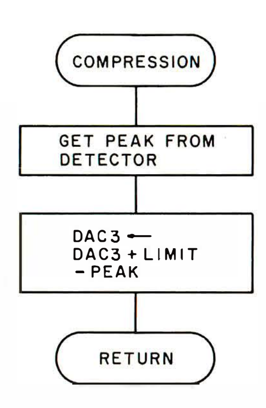


Figure 7: *Flowchart of a routine to perform compression of an audio signal. It adjusts the reference voltage of the input analog-to-digital converter to keep the output signal at a constant level. The assembler code for the 8080 processor is shown in listing 4.*

decreased. This action keeps the signal at a near constant level. Reaching the maximum possible gain of the analog-to-digital converter limits this action, thereby preventing noise from being amplified to audible levels in the absence of a signal.

Vibrato is obtained by using the algorithm shown in the flowchart of figure 8a. The 8080 code is shown in listing 5. This vibrato routine varies the amplitude of the audio signal approximately sinusoidally, with a period equal to eight times the interval between executions of this routine. To simulate a sine wave, the algorithm breaks one cycle into eight parts (0 thru 7, see figure 8b). Each time the routine executes, it fetches the offset value for that part of the curve from a look-up table. Different offset values are used for different levels of vibrato. The value obtained from the look-up table is then added to the reference voltage of the input digital-to-analog converter. The frequency of the vibrato is controlled by how often the routine executes.

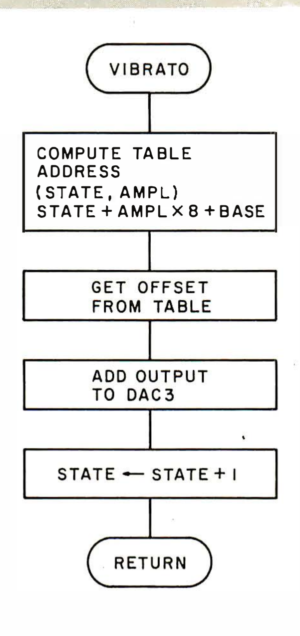
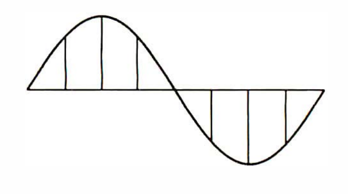


Figure 8a: *Flowchart of the vibrato routine. It varies the amplitude of the audio signal in an approximately sinusoidal manner by dividing a sine wave into eight discrete parts. Each time the routine executes, it fetches an offset value from a table for the present state and amplitude. This offset value is added to the reference voltage of the input digital-to-analog converter to produce the vibrato effect. The code is given in listing 5.*



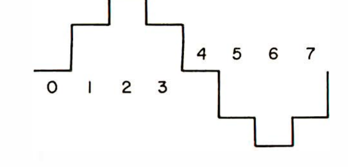


Figure 8b: *Division of the sine wave into eight parts and the resulting voltage levels for each state.*

```
VIBR:    LXI   H,AMPL      ;COMPUTE TABLE ADDRESS
         MOV   M,A         ;GET AMPLITUDE
         RAL               ;MULTIPLY BY 8
         RAL
         RAL
         INX   H           ;ADD TO STATE
         ADD   M           ;
         INR   M           ;INCREMENT STATE
         LXI   H,BASE      ;GET BASE ADDRESS
         ADD   L           ;ADD TO STATE + AMPL*8
         MOV   L,A
         LDA   DAC3IM      ;GET CURRENT VALUE OF VREF
         ADD   M           ;ADD TO TABLE OFFSET
         STA   DAC3        ;OUTPUT TO DAC
         RET               ;EXIT
```

Listing 5: *Routine to add vibrato coded for the 8080 processor. It uses table look-up of an 8-segment approximation of a sine curve to vary the input digital-to-analog converter (DAC) reference voltage. Figure 8a shows the flowchart.*

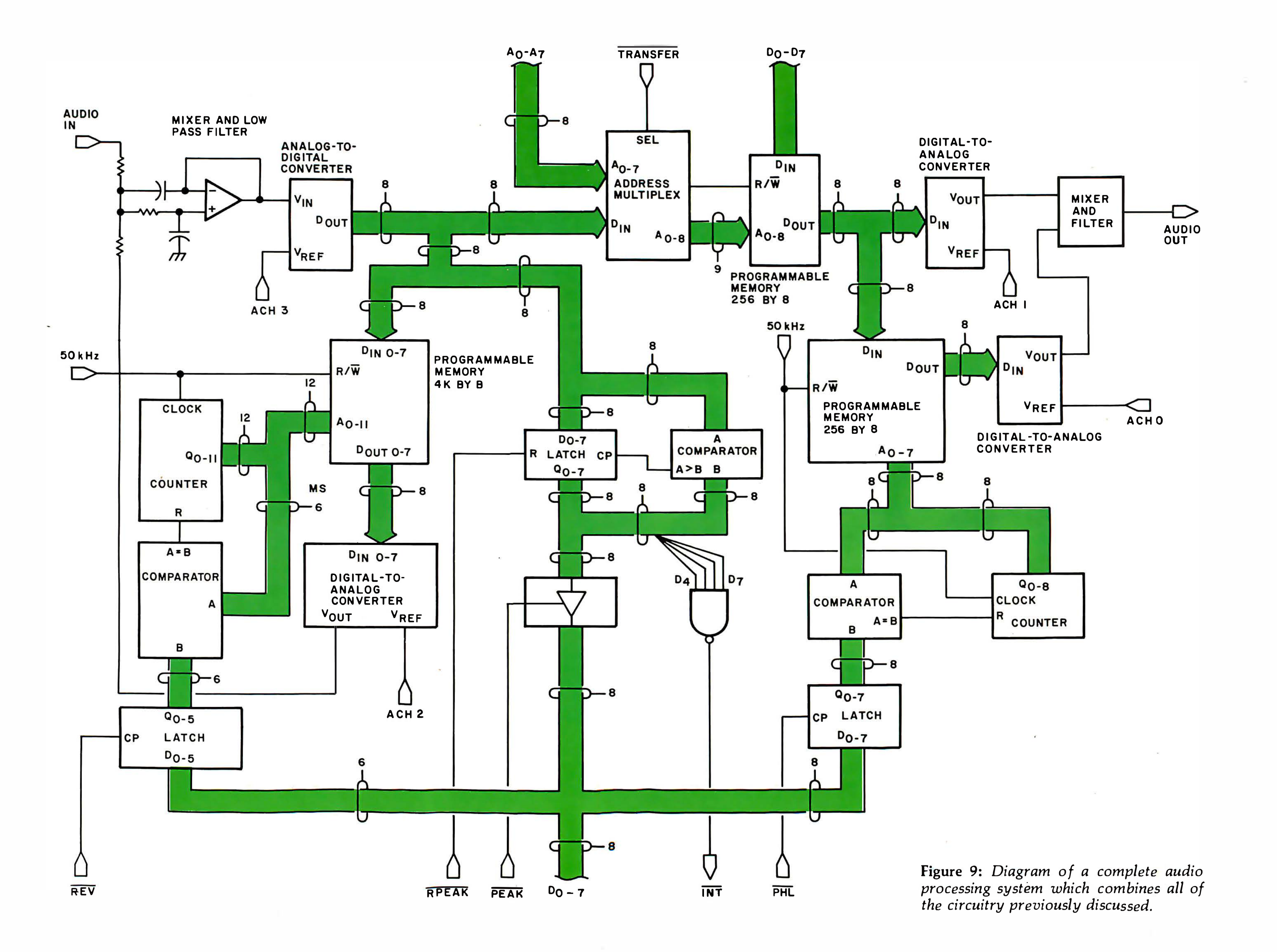


Figure 9: *Diagram of a complete audio processing system which combines all of the circuitry previously discussed.*

For a more precise sine wave, more states should be used to represent the curve. If the number of states is reduced, higher vibrato frequencies are possible. With eight states, the maximum vibrato frequency (with the routine executing once every ms) is 125 Hz. This is adequate for most applications. For even higher frequencies with less distortion, a voltage controlled oscillator may be added to the circuit.

The gain-control circuitry can also be used to minimize quantization noise by keeping the digital signals at near maximum levels and restoring their dynamics (amplitude variations) at the output digital-to-analog converter. However, care must be taken with this approach to restore the dynamics of delayed signals at levels that reflect the amplitude at the time that they were delayed.

Complete System

Combining the transfer, time-delay and gain-control functions into a single system saves money on hardware since all functions share the same analog-to-digital converter and processor, two of the most expensive components. Figure 9 shows a simplified diagram of the complete system which combines the circuitry described in all previous figures.

The system software is structured so that each function's routine should execute periodically, but each routine may execute with a different period. To control the calling of these function routines, the top level of the system software (shown in the flowchart of figure 10 and with code given in listing 6) is interrupt driven (by the frequency divider of figure 11), executing once every ms. This routine decrements software timers corresponding to each routine. When one of these timers reaches zero, the corresponding routine is called. On system power-up, all timers are initialized, and after executing a particular routine the timer corresponding to that routine is reinitialized.

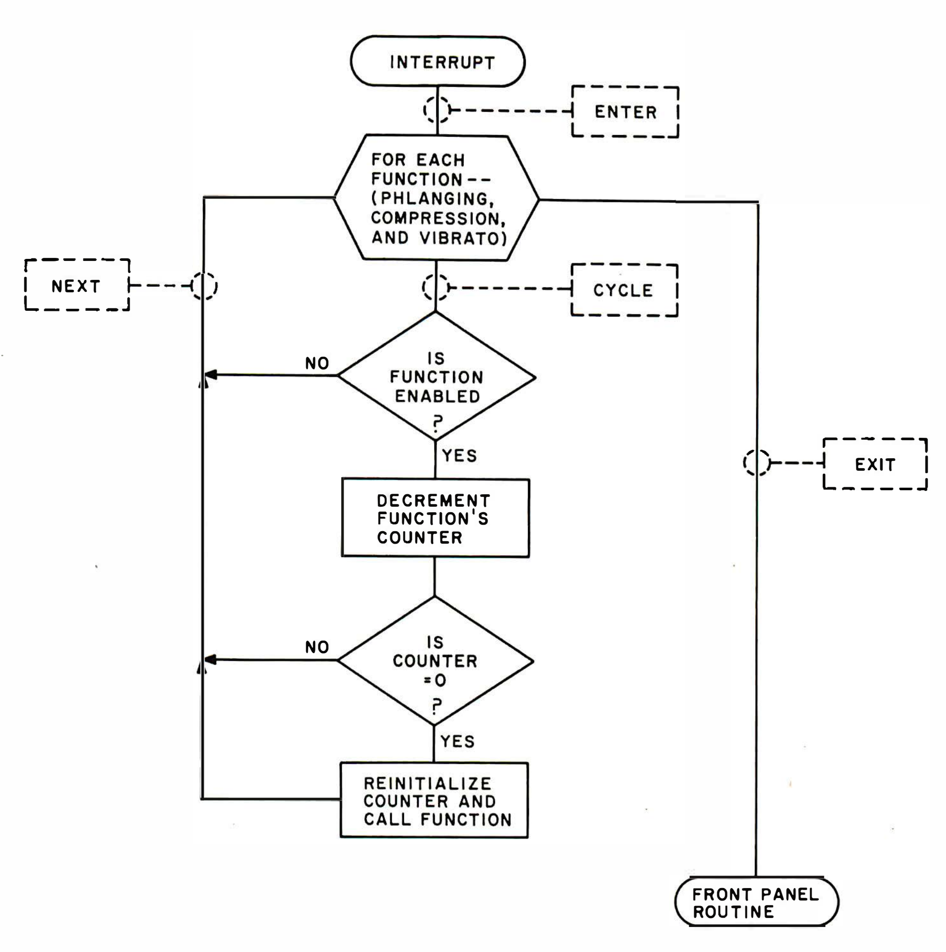


Figure 10: *Flowchart of the interrupt service routine. At intervals of 1 ms, an interrupt occurs from the real-time clock, and this interrupt service routine is executed. It calls the appropriate function routines at the proper times by decrementing software counters corresponding to each routine. When one of these counters reaches zero, its software routine is called and the time is reinitialized. If the function is not selected, the counter will not be decremented. The control panel service routine executes during any free time.*

```
INT:        LXI    D,ZPHLNG
            LXI    H,PLCNT      ;GET ADDRESS OF PHLANGE COUNTER
            MVI    B,3          ;3 FUNCTIONS PHLANGING,
;                               ;COMPRESSION AND VIBRATO
;                               ;FOR EACH FUNCTION
INTLP:      MOV    A,M          ;IS FUNCTION ENABLED
            CPI    FFH          ;?
            JZ     INT1         ;NO — NEXT FUNCTION
            DCR    M            ;YES — DECREMENT COUNTER
            PUSH   D            ;SAVE REGISTERS
            PUSH   H
            CZ     ZJMP         ;CALL ROUTINE IF ZERO
            POP    H            RESTORE REGISTERS
            POP    D
            INX    H            ;POINT AT NEXT FUNCTION'S
                                ;COUNTER
            INX    D            ;POINT AT NEXT
            INX    D            ;ENTRY IN JUMP
            INX    D            ;TABLE
            DCR    B            ;DECREMENT INDEX
            JNZ    INTLP        ;ITERATE IF NOT DONE
            RET                 ;EXIT IF DONE
;
ZJMP:       XCHG                ;GET ADDRESS OF ROUTINE
            PCHL                ;JUMP THROUGH TABLE
;
ZPHLNG:     JMP    PHLNG
ZCOMPR:     JMP    COMPR
ZVIBR:      JMP    VIBR
```

Listing 6: *The code for the interrupt service routine. The real-time clock causes this routine to be entered at intervals of 1 ms. It activates functions according to the proper schedule. Its flowchart is shown in figure 10.*

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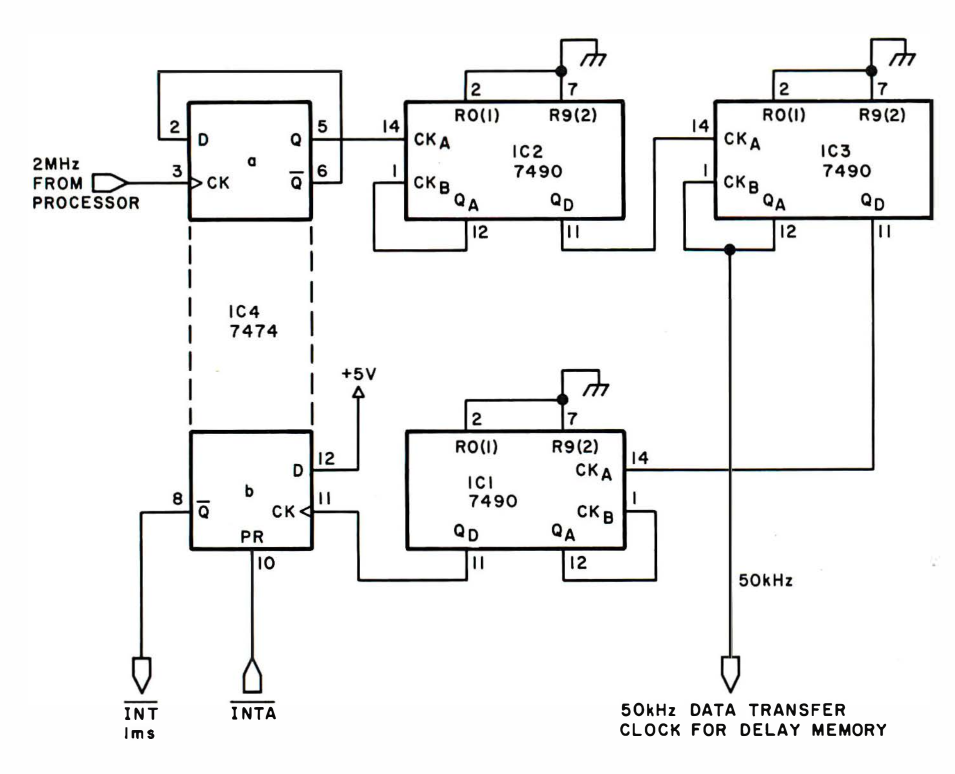


Figure 11: *Frequency divider for the 50 kHz data-transfer clock and the 1 ms real-time clock interrupt. The first stage divides the 2 MHz processor clock signal by forty, to obtain 50 kHz. This is further divided by fifty and sent to a flip-flop to interrupt the processor every 1 ms.*

Routines that execute once per ms are called on every interrupt and do not have timers. Any time left over at the end of the millisecond is used to service the control panel.

External User Control

The control panel used with the system (the device with which the user communicates with the system, selects functions, and specifies function parameters) can take many forms. A control panel can be as simple as a few toggle switches or as elaborate as a graphics terminal. The schematic diagram for a very simple control panel interface is shown in figure 12. Two pairs of seven-segment light emitting diode (LED) displays show the user which parameter is being observed and the value of that parameter. The value of the parameter can be adjusted by pressing increment or decrement switches. A parameter select switch changes the parameter displayed. The software to operate this panel is shown as a flowchart in figure 13, and the 8080 code is given in listing 7.

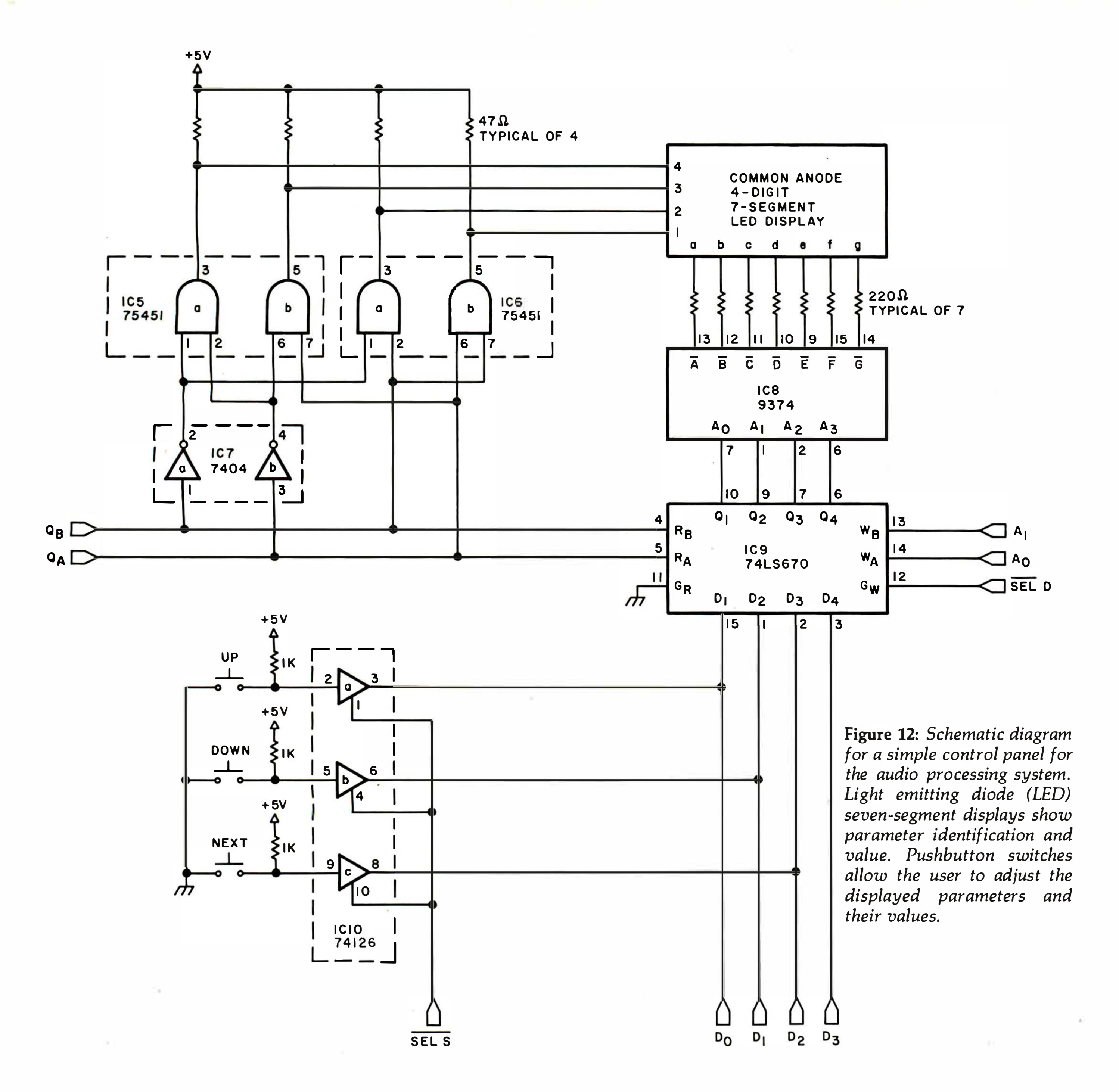


Figure 12: *Schematic diagram for a simple control panel for the audio processing system. Light emitting diode (LED) seven-segment displays show parameter identification and value. Pushbutton switches allow the user to adjust the displayed parameters and their values.*

This routine looks for transitions of the switches, and updates the display and parameters accordingly.

Conclusion

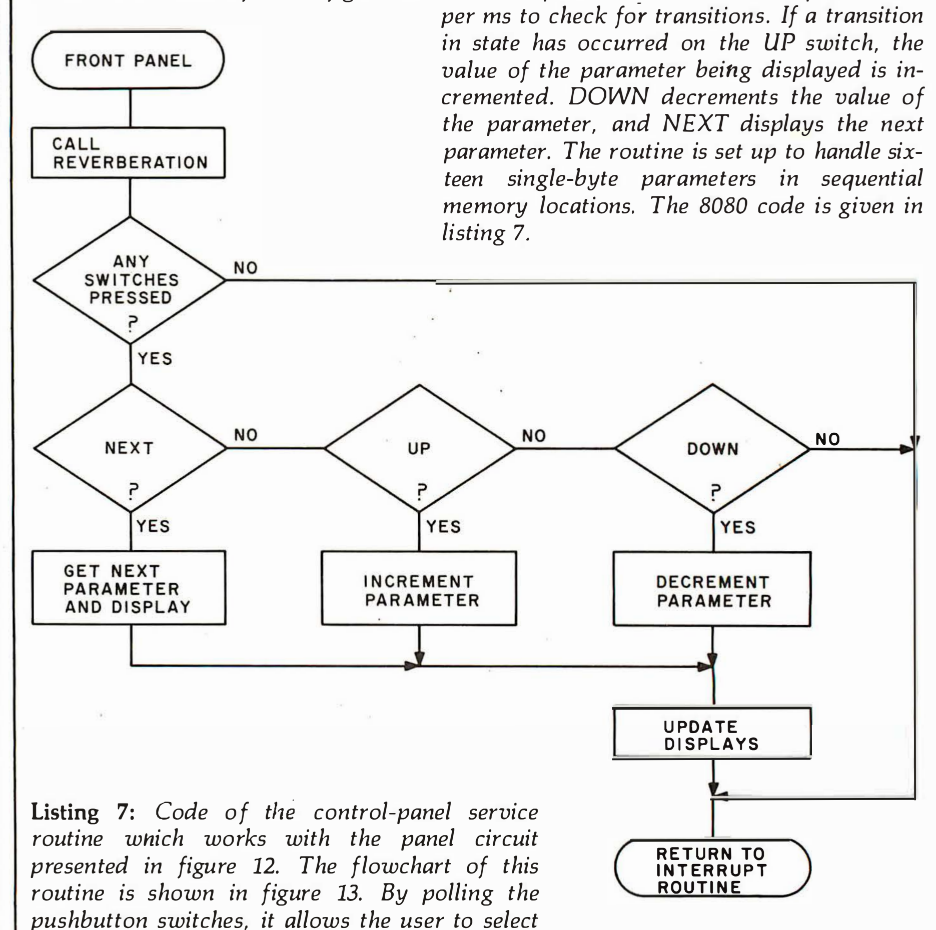
The interested user is by no means limited to the functions that I have described here. Tonal control, phase-shifting, and even synthesized chords are possible using digital techniques. Using a microcomputer, the possibilities are endless. The microcomputer can even generate the music it processes. There are certainly many unexplored instances where microcomputers can be applied to audio processing.

I have attempted to describe not only the design of one microcomputer audio processing system, but also the methodology used in designing *any* real-time microcomputer system. Before rushing into the design of a system, a top-down approach to the problem should be used, the system should be defined, a worst case timing analysis of the system should be performed and, if necessary, hardware versus software tradeoffs should be made to distribute tasks and allow reasonable execution times. An intelligent compromise between hardware and software is almost always the best solution.

Number	Type	+5 V	GND
IC1	7490	5	10
IC2	7490	5	10
IC3	7490	5	10
IC4	7474	14	7
IC5	75451	8	4
IC6	75451	8	4
IC7	7404	14	7
IC8	9374	16	8
IC9	74LS670	16	8
IC10	74126	14	7

Table 1: *Power supply connections for integrated circuits used in the designs described in this article.*

Figure 13: *Flowchart of the control-panel service routine. It supports the hardware shown in schematic form in figure 12. The three pushbutton switches are polled once per ms to check for transitions. If a transition in state has occurred on the UP switch, the value of the parameter being displayed is incremented. DOWN decrements the value of the parameter, and NEXT displays the next parameter. The routine is set up to handle sixteen single-byte parameters in sequential memory locations. The 8080 code is given in listing 7.*



Listing 7: *Code of the control-panel service routine which works with the panel circuit presented in figure 12. The flowchart of this routine is shown in figure 13. By polling the pushbutton switches, it allows the user to select function parameters and change their values. This routine is set up to handle sixteen single-byte parameters in sequential memory locations.*

```
FPR:     CALL  REVB      ;UPDATE REVERB
         LDA   PBSW      ;ANY BUTTONS PUSHED?
         ANI   7         ;MASK OFF UNUSED BITS, IF NO
                         ;BUTTONS PUSHED
         JZ    FPHLT     ;HALT AND WAIT FOR NEXT INTERRUPT
         MOV   B,A       ;AND SAVE DATA
         LXI   H,PBSIM   ;LOOK FOR TRANSITIONS
         CMA             ;
         ANA   M         ;IF 0 NOW AND WAS 1, TRANSITION
         JZ    FPHLT     ;EXIT IF NO TRANSITIONS
         MOV   M,B       ;ELSE UPDATE IMAGE
         LHLD  PARM      ;GET ADDRESS OF PARAMETER
         CPI   1         ;NEXT
         JNZ   UP        ;NO, CHECK UP
         MOV   A,L       ;GET LOW BYTE OF POINTER
         INR   A         ;YES, INCREMENT POINTER
         ANI   0FH       ;MODULO 16
         MOV   L,A       ;AND SAVE
         SHLD  PARM      ;
FPDIS:   MOV   A,M       ;GET NEW PARAMETER
         STA   PDISP     ;DISPLAY
         MOV   A,L       ;GET PARAMETER #
         STA   NDISP     ;DISPLAY
FPHLT:   HALT            ;HALT AND WAIT FOR INTERRUPT
UP:      CPI   2         ;UP?
         JNZ   DOWN      ;NO — GO CHECK DOWN
         INR   M         ;YES — INCREMENT PARAMETER
         JMP   FPDIS     ;AND DISPLAY

DOWN:    CPI   4         ;DOWN?
         JNZ   FPHLT     ;NO — HALT
         DCR   M         ;YES — DECREMENT PARAMETER
         JMP   FPDIS     ;AND DISPLAY ■
```

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Problems 1 thru ten

Most publications other than BYTE print "two," not "2" in the midst of an English sentence. Now when I read BYTE I have to go through a kind of mental stuttering: "2, oh yes, that means *two*." It is the same sort of gear shifting I go through whenever I read text that says "hopefully" when "I hope" is meant, or spells "through" as t, h, r, u, as the Chicago *Tribune* used to do. These are all examples of manner interfering with matter.

I do not object to *all* reforms in communication (going metric suits me fine), but this one is unrewarding.

Philip Bacon
3101 NW 2nd Ave
Gainesville FL 32607

The road to truth and beauty is sometimes a convoluted one. You will notice that our humorous experiment with simplistic rules only lasted for an issue or two — and that reason and judgement have now prevailed. We resolve 1 [sic] thing at a time. . . . CTH

S-100 Core?

I have an S-100 bus computer and would like to install core memory in it. I have been unsuccessful in locating anyone marketing such a device. I would greatly appreciate any information on the subject.

If no one is manufacturing S-100 core, where might I locate core planes that I can interface to the S-100 bus?

Larry Smith
R and L Enterprises
2901 Willens Dr #6
Melrose Park IL 60164

Removing Solder — A Comment

William Trimmer's article "Soldering Techniques" (September 1979 BYTE, page 84) covers the basics of soldering very well, but I would like to take exception to his suggestion to remove solder by "Rap(ping) the edge of the board smartly on the workbench." This practice could crack the board at worst, or the flying solder could bridge across the foil patterns, causing a short.

My technique for desoldering is to take "Solder-Wick," dip it in liquid rosin flux and wick up the solder as Mr. Trimmer mentions in his article. I find that the liquid flux improves the wicking action of the braid.

John F Roystone
4084A Birch Ct
Shaw AFB SC 29152

Weather Radio Information

There seems to be a request for information relating to Weather Satellite Receiving Equipment.

I have had a receiving set in operation since the fall of 1973, using a modified Heathkit GR-110 as a receiver, and using other ideas from the NASA SP 5079.

A much more informative and practical book is *Weather Satellite Handbook*, by Dr Ralph E Taggart of Michigan State University.

C A Bush
5538 Larch St
Vancouver British Columbia
V6M 4E1 CANADA

Subroutine Parameters Questioned

With all due respect to Professor Maurer, his D(L,L) example in "Subroutine Parameters" (July 1979 BYTE, page 228) would *always* yield strange results, without regard to the particular parameter passing technique employed. If the function of D is to zero the first parameter while doing nothing with the second, calling it with the same actual parameter in both places is a logical inconsistency, demanding that the same thing be made zero and be left alone simultaneously. The CDC 6400 program did not "work" any better than the IBM one; it simply produced a *different* "strange" result, which the programmer apparently found more acceptable.

I also question, on page 230, the statement that the $S = S + X$ example will not work with call-by-reference. Again, the problem here appears to be inherent in the logic of the case. The logic of the subroutine is expected to do $S = S + A(I)$ on the range $I = 1,10$, while at the

same time treat the formal parameter X as standing for a simple variable. I am not familiar with ALGOL 60, but most FORTRANs handle the situation by requiring an array declaration for X in the body of the subroutine's code.

Omri Serlin
POB 62138
Sunnyvale CA 94086

WD Maurer Replies:

When we CALL D(A,B), where D is defined by SUBROUTINE D(X,Y), the basic idea is that X is "really" A and that Y is "really" B. Any time we see an X in the subroutine D, we expect it to stand for A, in the context of this particular call. If, for example, we set X to U and then Y to V, that corresponds to setting A to U and B to V. If A and B are really both the same variable L, then we have set L to U and then L to V, which is perfectly acceptable. If we have set X to U and not set Y to anything, then, if the actual parameters are both L, we should set L to U. The fact that we have not set Y to anything does not *mean that the old value of L should necessarily be preserved without modification, since there are many other possible ways that the variable L can have another name; for example, it can be in COMMON, referenced by both D and the program which calls D.*

The second of Mr Serlin's concerns is a simple matter of confusion about ALGOL 60. If I put S = S + X in a loop in ALGOL 60, it is capable of doing S = S + A[1] the first time, S = S + A[2] the second time, etc, through the loop. If I put S = S + X in a loop in FORTRAN, it must *add the same* quantity *X each* time *through the loop. In this case it will be A(*i*), where* i *was the value that the variable I takes on when the subroutine is entered. Requiring an array declaration for X would make X into an array name, in which case S = S + X would not be syntactically valid.*

W D Maurer
George Washington University
SEAS
Washington DC 20052

Quest Comments

Thanks so much for the QUEST program listed in the July 1979 BYTE. As novices, it was fun modifying this routine to run on our TRS-80.

By placing personal references in some of the maze locations, our family has received hours of fun, often late into the night.

For any beginners who wish to do more than buy cassette games, listings such as this are well worth a BYTE subscription.

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Technical Forum

A Proposed Graphics Software Standard
Part 2

Dr Vincent C Jones, 1913 Sheely Dr, Ft Collins CO 80526

Sample Implementation

In part 1, the framework for a proposed graphics software standard was discussed.

An implementation of the 8080 assembly language protocol for use with the Cromemco Dazzler (listing 1) illustrates how the algorithms and standards presented translate into working software. Except for a few instances where the architecture of the 8080 or Dazzler allowed substantial simplification, the program code corresponds exactly to the Nassi-Schneiderman charts in part 1. The major deviations are in the handling of control characters in the routine CHAR, affected byte address calculation in DOT, and the termination condition in PAGE.

The software starts by defining the standard entry points. The Dazzler is assumed to be jumpered to use ports 16 and 17 (octal), the Cromemco default. If you own a Dazzler and it uses different ports, the I/O (input /output) commands in INITG, CHAR, and ANIMAT will need modification.

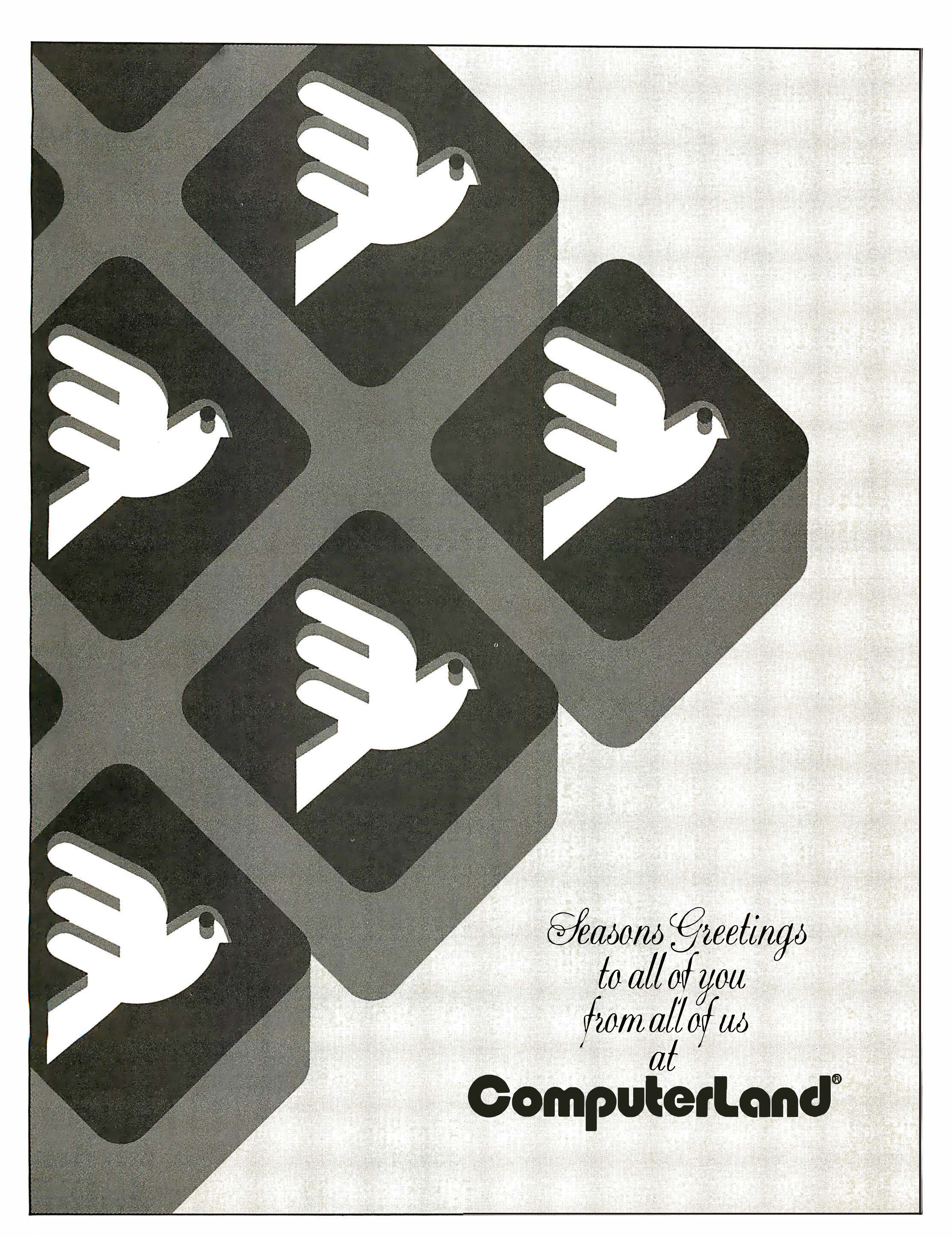
8080/Dazzler INITG

The first step in all these routines is to preserve any registers affected. In this case, HL is not saved because its contents will be replaced by the display description parameters.

The Dazzler requires the refresh buffer to start at an even multiple of 512. No test is made to check and see if the address provided is valid; instead, an algorithm that converts any address to a valid address and a valid address to itself is used. The refresh buffer address calculated is then stored in the two bytes labeled RBUF. Placing all the variables in a single section of memory is not only good programming practice, it also permits efficient setting of defaults by using register indirect addressing. The call to the CHAR routine with zero accumulator sets the display mode to MAXR and takes care of outputting the required controls to the Dazzler's Color/Mode port.

After calling PAGE to clear the screen, the Dazzler is finally turned on. The high-byte of the refresh buffer address is retrieved from memory and rotated into the bit position expected by the Dazzler. The OUT instruction starts the display, if it is not already on. The final step, before restoring register values, is to load the appropriate parameter description into HL. Hexadecimal 8AFC indi-

Text continued on page 176
Listing on page 84



Circle 75 on inquiry card.

Listing 1: *Implementation of the 8080 assembly language protocol for use with the Cromemco Dazzler. With a few exceptions, the program corresponds exactly to the Nassi-Schneiderman charts in part 1.*

```
                  ;          THE VCJ GRAPHICS PACKAGE
                  ;            8080/DAZZLER VERSION
                  ;        VERSION 3.02B  <>  AUG 25, 1977
                  ;
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                  ;     *  MODIFICATION OR ADAPTATION FOR  *
                  ;     *  PERSONAL USE IS PERMITTED PRO-  *
                  ;     *  VIDED THIS NOTICE IS INCLUDED.  *
                  ;     *                                  *
                  ;     ************************************
                  ;
                  ;
                  ;JUMP TABLE TO DEFINE STANDARD ENTRY POINTS
                  ;
0104                      ORG     104H     ;START OF STANDARD SPACE
0104 C31901               JMP     INITG    ;INITIIALIZE GRAPHICS
0107 C34501               JMP     PAGE     ;CLEAR THE SCREEN
010A C35901               JMP     CURSOR   ;GO TO A POINT ON THE SCREEN
010D C37701               JMP     DOT      ;DISPLAY A POINT ON THE SCREEN
0110 C3F101               JMP     LINE     ;DRAW A LINE BETWEEN POINTS
0113 C38F02               JMP     CHAR     ;DISPLAY AN ASCII CHARACTER
0116 C38F03               JMP     ANIMAT   ;CHANGE BUFFERS WITHOUT FLICKER

                  ;DEFINE THE DAZZLER PORTS
000E =            DAZ0    EQU     0EH      ;CONTROL PORT
000F =            DAZ1    EQU     DAZ0+1   ;COLOR/MODE PORT

                  ;
                  ;ROUTINE INITG
                  ;       INITIALIZE THE DAZZLER TO 128 BY 128 B/W MODE,
                  ;          X = 0, Y = 0, SCREEN CLEARED, AND
                  ;          CURRENT COLOR SET TO WHITE.
                  ;       H,L CONTAINS THE FIRST AVAILABLE ADDRESS
                  ;          FOR REFRESH BUFFERS.
                  ;       RETURNS DISPLAY CHARACTERISTICS IN H,L
                  ;
0119 F5           INITG:  PUSH    PSW      ;SAVE A FEW REGISTERS
011A D5                   PUSH    D        ;
011B 2B                   DCX     H        ;FIX REFRESH ADDR TO LEGAL
011C 7C                   MOV     A,H      ;   BOUNDARY
011D C602                 ADI     02H      ;
011F E6FE                 ANI     0FEH     ;CLEAR 256 BIT
0121 67                   MOV     H,A      ;
0122 AF                   XRA     A        ;CLEAR A
0123 6F                   MOV     L,A      ;  AND MAKE LOW BYTE ZERO
0124 22A904               SHLD    RBUF     ;SAVE BUFFER ADDRES
0127 21AB04               LXI     H,ANIM   ;START OF VARIABLE AREA
012A 77                   MOV     M,A      ;FILLING BUFFER 0
012B 23                   INX     H        ;REAIM AT YPOS
012C 77                   MOV     M,A      ;   WHICH IS ZERO
012D 23                   INX     H        ;REAIM AT XPOS
012E 77                   MOV     M,A      ;  WHICH IS ZERO
012F 23                   INX     H        ;REAIM AT CURRENT COLOR
0130 36FF                 MVI     M,0FFH   ;  WHICH IS WHITE
0132 CD8F02               CALL    CHAR     ;128 BY 128 MAX RESOLUTION MODE
0135 CD4501               CALL    PAGE     ;AND FINALLY A CLEAR SCREEN
0138 3AAA04               LDA     RBUF+1   ;RETRIEVE REFRESH ADDRESS
013B 37                   STC              ;FUTURE ON BIT
013C 1F                   RAR              ;NOW HAVE A DAZZLER CONTROL
013D D30E                 OUT     DAZ0     ;SO TURN IT ON
013F 21BC8A               LXI     H,8ABCH  ;DISPLAY DESCRIPTION
0142 D1                   POP     D        ;RESTORE REGISTERS
0143 F1                   POP     PSW      ;
0144 C9                   RET              ;ALL DONE

                  ;
                  ;ROUTINE PAG
                  ;       CLEAR THE SCREEN
                  ;          OR CLEAR 2K OF MEMORY COMMENCING
                  ;         AT THE ADDRESS IN 'RBUF'.
                  ;
0145 F5           PAGE:   PUSH    PSW      ;SAVE THE USER WORLD
0146 D5                   PUSH    D        ;
0147 E5                   PUSH    H        ;
0148 2AA904               LHLD    RBUF     ;STARTING ADDRESS
014B 3E08                 MVI     A,08H    ;(BUFFER LENGTH/256)
014D 84                   ADD     H        ;HIGH BYTE OF LAST ADDR +1
014E 5D                   MOV     E,L      ;NEED A ZERO FOR MEMORY FILL
014F 73           P000:   MOV     M,E      ;ZAP THAT BYTE
0150 23                   INX     H        ;NEXT BYTE
0151 BC                   CMP     H        ;DONE YET?
0152 C24F01               JNZ     P000     ;NO.  KEEP TRUCKING
0155 E1                   POP     H        ;RESTORE THE USER
0156 D1                   POP     D        ;
0157 F1                   POP     PSW      ;
0158 C9                   RET              ;ALL DONE

                  ;
                  ;ROUTINE CURSOR
                  ;       POSITION THE CURSOR AT X,Y IN H,L
                  ;          OR CONVERT THE COORDINATES IN H,L FROM
                  ;             STANDARD COORDINATES (0-255 ON EACH AXIS)
                  ;             TO THE COORDINATES CURRENTLY IN USE BY THE
                  ;             DAZZLER.
                  ;
0159 F5           CURSOR: PUSH    PSW      ;SAVE THE WORLD
015A E5                   PUSH    H        ;  OR AT LEAST PART
015B CD6401               CALL    CU000    ;CONVERT TO COORD IN USE
015E 22AC04               SHLD    YPOS     ;AND SAVE FOR OTHER PEOPLE
0161 E1                   POP     H        ;RESTORE THE WORLD
0162 F1                   POP     PSW      ;
0163 C9                   RET              ;ALL DONE

                  ;INTERNAL SUBROUTINE CU000
                  ;       CONVERT THE X,Y COORDINATE PAIR IN H,L TO
```

Listing 1 continued:

```
                       ;          THE COORDINATE SYSTEM CURRENTLY IN USE
                       ;
                       ;      USES REGISTERS A, H, AND L
                       ;
0164 3AAF04            CU000:  LDA     MODE      ;WHICH MODE?
0167 F5                CU001:  PUSH    PSW       ;WILL NEED IT LATER
0168 AF                        XRA     A         ;MOVE H TO A WITH CY CLEAR
0169 B4                        ORA     H
016A 1F                        RAR               ;DIVIDE BY 2
016B 67                        MOV     H,A       ; AND SAVE IT
016C AF                        XRA     A         ;DO THE SAME FOR Y
016D B5                        ORA     L
016E 1F                        RAR
016F 6F                        MOV     L,A       ;ALL DONE IF 128 BY 128
0170 F1                        POP     PSW       ;WHAT MODE ARE WE IN?
0171 3C                        INR     A         ; 128 BY 128?
0172 F0                        RP                ;YES, ALL DONE
0173 AF                        XRA     A         ;64 BY 64, PRETEND 128
0174 C36701                    JMP     CU001     ;  AND DIVIDE AGAIN

                       ;ROUTINE DOT
                       ;      DISPLAY THE POINT AT THE CURSOR POSITION
                       ;
                       ;BLOCK #1:  ADDRESS CALCULATION FROM Y POSITION
                       ;
0177 F5                DOT:    PUSH    PSW       ;SAVE THE WORLD
0178 C5                        PUSH    B         ;
0179 D5                        PUSH    D         ;
017A E5                        PUSH    H         ;
017B 3AAF04                    LDA     MODE      ;GET THE DISPLAY MODE BYTE
017E 4F                        MOV     C,A       ;00=MAXR,80=MAXC,01=R128,81=R64
017F 3AAC04                    LDA     YPOS      ;Y ADDR IS FIRST
0182 0C                        INR     C         ;WHICH RESOLUTION
0183 FA8801                    JM      D101      ;64 BY 64
0186 F5                        PUSH    PSW       ;SAVE FOR BIT MASK TIME
0187 1F                        RAR               ;DIVIDE BY 2
0188 2F                D101:   CMA               ;CONVERT TO LINE NUMBER
0189 57                        MOV     D,A       ;SAVE A COPY
018A E61F                      ANI     1FH       ;EACH QUADRANT IS 32 HIGH
018C 6F                        MOV     L,A       ;MULT LINE # BY BYTES/LINE
018D 7A                        MOV     A,D       ;BUT FIRST CORRECT FOR QUADRANT
018E E620                      ANI     20H       ;WHICH ARE WE IN?
0190 CA9701                    JZ      D102      ;1ST OR 2ND, NO CORRECT REQ
0193 3E40                      MVI     A,40H     ;MOVE DOWN TO 3RD OR 4TH
0195 85                        ADD     L         ;WHICH IS 1K AFTER SHIFTING
0196 6F                        MOV     L,A       ;END OF QUADRANT CORRECTION
0197 2600              D102:   MVI     H,00H     ;READY TO MULTIPLY BY 16
0199 29                        DAD     H         ;TIMES 2
019A 29                        DAD     H         ;TIMES 2
019B 29                        DAD     H         ;TIMES 2
019C 29                        DAD     H         ;TIMES 2 = TIMES 16
019D EB                        XCHG              ;MAKE ROOM FOR BASE ADDRESS
019E 2AA904                    LHLD    RBUF      ;WHERE DO WE START?
01A1 19                        DAD     D         ;H,L IS FIRST BYTE ON LINE
                       ;
                       ;BLOCK #2:  ADDRESS CALCULATION FROM X POSITION
                       ;
01A2 3AAD04                    LDA     XPOS      ;GET X CURSOR
01A5 0C                        INR     C         ;WHICH RESOLUTION?
01A6 FAAB01                    JM      D201      ;64 BY 64
01A9 F5                        PUSH    PSW       ;128 BY 128, SAVE FOR BLOCK #3
01AA 1F                        RAR               ;DIVIDE BY 2
01AB 57                D201:   MOV     D,A       ;SAVE FOR LATER
01AC E620                      ANI     20H       ;CHECK QUADRANT
01AE CAB501                    JZ      D202      ;QUAD 1 OR 3, NO CORRECTION
01B1 3E02                      MVI     A,02H     ;QUAD 2 OR 4, ADD 512
01B3 84                        ADD     H         ; TO GET CORRECT ADDRESS
01B4 67                        MOV     H,A       ;QUADRANT CORRECTION COMPLETE
01B5 7A                D202:   MOV     A,D       ;X CURSOR (NORM 64)
01B6 E61E                      ANI     1EH       ;32 TO A QUADRANT
01B8 0F                        RRC               ;2 POINTS PER BYTE
01B9 5F                        MOV     E,A       ;  ADD TO LINE ADDRESS
01BA 7A                        MOV     A,D       ;  BUT SAVE COPY OF 64 VALUE
01BB 1600                      MVI     D,00H     ;CLEAR D FOR A DOUBLE ADD
01BD 19                        DAD     D         ;NOW HAVE THE BYTE ADDRESSED
                       ;
                       ;BLOCK #3:  BIT MASK GENERATION
                       ;
01BE 1F                        RAR               ;EVEN OR ODD?
01BF 3E0F                      MVI     A,0FH     ;ASSUME EVEN
01C1 D2C501                    JNC     D301      ;CORRECT ASSUMPTION
01C4 2F                        CMA               ;WAS ODD, SWITCH HALVES
01C5 0C                D301:   INR     C         ;128 BY 128?
01C6 FAE201                    JM      D400      ;64 BY 64!
01C9 57                        MOV     D,A       ;SAVE MASK
01CA F1                        POP     PSW       ;XPOS
01CB E601                      ANI     01H       ;EVEN OR ODD?
01CD 5F                        MOV     E,A       ;SAVE LOW BIT
01CE F1                        POP     PSW       ;YPOS
01CF 1F                        RAR               ;EVEN OR ODD?
01D0 3E33                      MVI     A,33H     ;ASSUME ODD
01D2 DAD601                    JC      D302      ;VALID ASSUMPTION
01D5 2F                        CMA               ;NO, EVEN
01D6 A2                D302:   ANA     D         ;DOWN TO 2 BITS
01D7 1D                        DCR     E         ;FINALLY DO X
01D8 CAE001                    JZ      D303      ;X WAS ODD
01DB E655                      ANI     55H       ;X WAS EVEN
01DD C3E201                    JMP     D400      ;
01E0 E6AA              D303:   ANI     0AAH      ;X WAS ODD
                       ;
                       ;BLOCK #4:  REFRESH MEMORY MODIFICATION
                       ;
01E2 57                D400:   MOV     D,A       ;SAVE THE BIT MASK
01E3 2F                        CMA               ;FIRST ERASE ORIGINAL CONTENTS
01E4 A6                        ANA     M         ;
01E5 5F                        MOV     E,A       ;SAVE CLEANED VERSION
01E6 3AAE04                    LDA     COLOR     ;GET COLOR DESIRED
01E9 A2                        ANA     D         ;DOWN TO DESIRED POINT
01EA B3                        ORA     E         ;ADD TO ORIGINAL CONTENTS
01EB 77                        MOV     M,A       ;AND STUFF INTO MEMORY
01EC E1                D402:   POP     H         ;RESTORE THE WORLD
01ED D1                        POP     D         ; NOTE: THIS SERIES IS
01EE C1                        POP     B         ;   ALSO USED BY LINE
01EF F1                        POP     PSW       ;   AND CHAR.
01F0 C9                        RET               ;ALL DONE

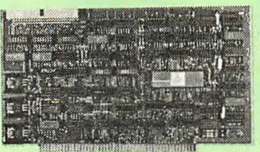
                       ;
                       ;
```

Listing 1 continued on page 168

DELTA IS READY . . .

WITH

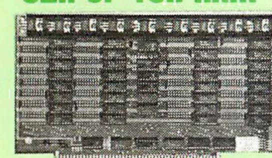
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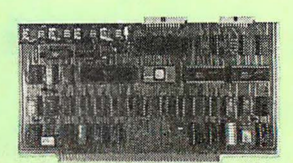
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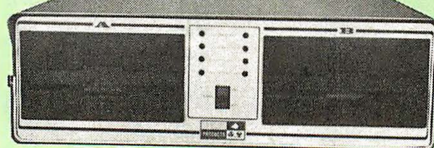
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Relative Subroutines for the Z80

Dennis Bathory Kitsz, Roxbury VT 05669

One of the problems associated with writing versatile, relocatable programs for microprocessors is making decisions on how to use subroutines. The main difficulty occurs when a program using subroutines is to relocate itself; every call address must be rewritten. On the other hand, avoiding subroutines wastes valuable memory space.

I faced this dilemma when developing a program to exercise the memory in my TRS-80; a bit had failed, and I needed a program that could reside in low-memory during a test of high-memory, and relocate itself to high-memory in order to test low-memory. The lengthy process had to be repeated many times (preferably while I was asleep), and leave the results displayed on the monitor the next morning. The necessary ingredients for this program were: a test of all combinations of bits in a byte; a section to identify the bad address; hexadecimal and ASCII conversion routines; a clear-screen and address display routine; and a section to relocate the program and display that fact. A further requirement was that the program reside in a single page of memory.

The identification for each bad address was written as a subroutine; nested inside were the conversions to hexadecimal and ASCII and the display section. Altogether, six separate subroutine calls were needed to identify and display each faulty address.

Self-relocation of the program could have ended with a flurry of activity, transferring the program and rewriting every CALL with a specific new address.

Instead, it was possible to write the program with "relative" subroutines which are not address-specific. This concept is not entirely new, and some late-generation processors employ many such position-independent commands. However, the current crop of popular chips does not offer any direct way of accessing a nearby subroutine. The following procedure illustrates one way it can be achieved with the Z80:

- determine the offset from the end of the subroutine back to the main program flow;
- assign this value as the operand of a relative jump placed at the end of the subroutine;
- jump to the subroutine.

Here is an example of a "relative call and return" situation — and it uses only two bytes more than a standard subroutine:

```
1000    LD IX,1080        ;CENTER POINT OF ONE PAGE
1004    [MAIN PROGRAM]
          .
          .
          .
1040    LD (IX+8),BD      ;IDENTIFY RETURN OFFSET AND
                           PUT IN PLACE
1044    JR 20             ;JUMP TO THE SUBROUTINE
1046    [MAIN PROGRAM]
          .
          .
          .
1066    [SUBROUTINE]
          .
          .
          .
1087    JR XX             ;RETURN TO MAIN PROGRAM
                           FLOW
```

Note that, like an absolute subroutine, this configuration may be entered at any point — only the offset value loaded into the return jump must change.

In the case of a conditional return, moreover, the circumstances gain only one step in complexity, as the return value cannot be determined by the main program before the subroutine is executed. Instead, whenever a return condition is met during subroutine execution, the conditional jump transfers control to the last instruction of the subroutine, which is the "loaded" jump. It then returns to the main program flow.

Both these procedures have one characteristic that many programmers tend to avoid, and that is their self-modifying activity. Naturally, this obviates their use in read-only memory. But if it is important to have a relocatable module, it can be achieved with only one register (IX or IY) needing a specific address.

The memory use benefits of either method can be determined quickly. If it takes 5 bytes to rewrite an address directly, and a standard CALL and return combination needs 4 bytes, then a 6-byte unconditional or an 8-byte conditional "relative call" is the obvious choice. Overall, these methods provide an efficient and versatile escape from the usual complexities of creating relocatable programs. ■

APL/S: An Alternative

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About the Author
Robert G Brown is an independent consultant after having worked for IBM for 13 years. He began using APL in 1968 and structured programming in 1970. When he designed the APL/S language in 1978, he attempted to combine structured programming with APL on a small computer in a way which removes some of the common objections to both.

APL/S is a modified subset of APL plus structured-programming control figures. It is intended to be a good first language both for those who may go on to more powerful languages such as Pascal or APL, and for those whose computational needs are destined to remain modest.

Pseudocode

Structured programming is a collection of techniques that help produce demonstrably correct programs. One of the fundamental ideas is to first state the action of the program in what is sometimes called *pseudocode*, or structured English, then progressively refine the statements of the program toward the programming language being used.

With structured English, any imperative statement can be used, but alternation and repetition statements are restricted to a few well defined forms. In this case, the forms are IF-THEN-ELSE, ENDIF for alternation and WHILE-DO, ENDWHILE for repetition. Their intuitive meaning can be illustrated by a set of dieting instructions.

The instructions are to keep eating, one byte at a time, as long as you are hungry. When you are no longer hungry, ask yourself whether you want to get fat. If you do, eat some more. A structured English statement of these instructions is:

```
WHILE you are hungry
DO eat a byte
ENDWHILE
IF you want to get fat
THEN eat some more
ENDIF
```

An APL/S Program

The pseudocode for a guess-the-number-game program is shown in listing 1a. The input is a series of guesses at a

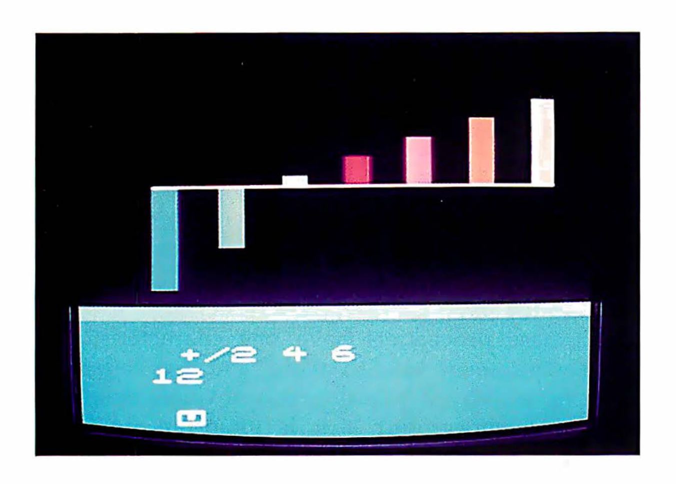


Photo 1: *An immediate-mode calculation displayed on an ordinary television set. The user entered "+/2 4 6". This expression was evaluated, and the result (12) was displayed. The +/ characters indicate that the elements of the array 2 4 6 should be added. Therefore 2+4+6 gives 12 as the result. The cursor (an inverse video U, which shows up as a white square with a U inside) indicates that the keyboard is open for the next immediate-mode entry. The histogram bars are left over from a previous calculation.*

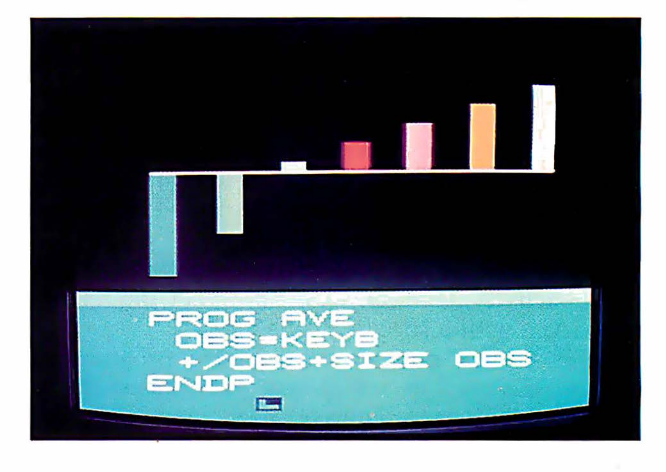


Photo 2: *Program AVE, which computes the average of a set of numeric observations. Input is from the keyboard as a series of numeric values — an array constant. The input, returned by the KEYB function, is assigned to OBS, thus making OBS an array. The average value is computed by adding up the elements of the array (+/OBS) and dividing the sum by the size of the array (SIZE OBS). Since the result is not assigned to a variable, it is displayed.*

Listing 1a: *Pseudocode for a guess-the-number-game program. This type of expression may be called Structured English. See listing 1b for the APL/S equivalent.*

```
Pick a number between 1 and 100
Set the number of guesses to 1
WHILE the guess from the keyboard is not equal
  to the number picked
DO add 1 to the number of guesses
    IF the guess is higher than the number
    THEN display "Too high"
    ELSE display "Too low"
    ENDIF
    Display "Try again"
ENDWHILE
Display "Number guesses-"
Display the number of guesses
```

randomly selected number. The outputs are messages saying "too high," "too low," and "try again." When the number is correctly guessed, the number of guesses made is displayed.

The corresponding APL/S program, named GUESS, is shown in listing 1b. It is a line-for-line translation of the pseudocode. By looking at the pseudocode and the sample execution in listing 2, the programmer should be able to understand the main points of the APL/S program, although all the details may not be clear.

A Description of APL/S

A more complete and precise description of APL/S is provided by the syntax diagrams in figure 1 thru 5 and

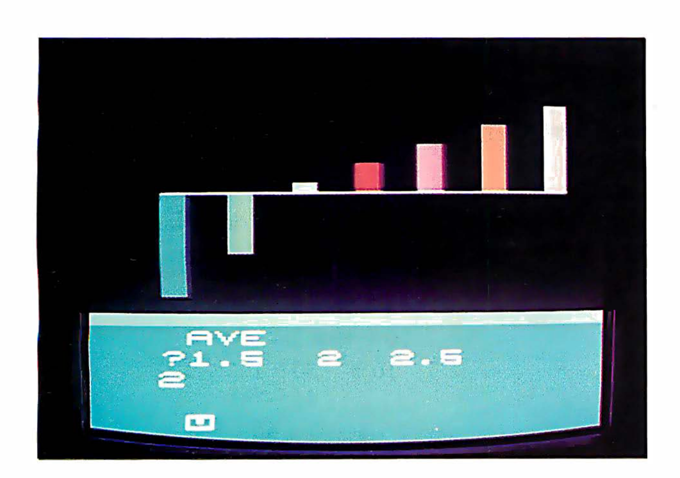


Photo 3: *The program AVE is executed by keying in its name. Keyboard input is prompted by a question mark (?). The user entered the 3-element array constant 1.5 2 2.5. In the program, +/OBS÷SIZE OBS was evaluated as +/OBS (giving 6) divided by SIZE OBS (giving 3) for a result of 2.*

Listing 1b: *APL/S program for the guess-the-number game. In this implementation of the language, keywords such as PROGRAM and RANDOM may be abbreviated by the first four letters. See listing 2 for an example of the execution of this routine.*

```
PROGRAM GUESS
    NUM=RANDOM 100
    NGES=1
    WHILE NUM NE GES=KEYB
    DO NGES=NGES+1
        IF GES GT NUM
        THEN "TOO HIGH"
        ELSE "TOO LOW"
        ENDIF
        "TRY AGAIN"
    ENDWHILE
    "NUMBER GUESSES-"
    NGES
ENDPROGRAM
```

Listing 2: *Example execution of the program of listing 1b. Execution of a program is started by typing the name of the program, in this case GUESS. User input is prompted by a question mark (?) character.*

```
 GUESS
?50
TOO HIGH
TRY AGAIN
?25
TOO LOW
TRY AGAIN
?32
NUMBER GUESSES-
3
```

the function descriptions in table 1. Starting at the diagram labeled Program, a path through the diagrams defines a syntactically correct APL/S program. The diagrams do not specify APL/S *action* (that is, the meaning or semantics of the program).

Each circle indicates a *terminal symbol*. Terminal symbols become part of the program text exactly as shown. The boxes indicate *nonterminals*. For each nonterminal there is a diagram (or, for functions, a description in table 1). When all nonterminals have been replaced with sequences of terminals according to the diagrams (or table 1), the result is a syntactically correct APL/S program.

The syntax diagrams in figures 1 thru 5 do not cover statements for loading, saving, editing, or tracing the execution of programs. A complete description of APL/S can be found in the paper "An Introduction to APL/S" (part of the *Conference Proceedings of the Third West Coast Computer Faire*, November 1978) and the *APL/S User's Manual* by W Judd and S Cintz (available from the VideoBrain Computer Co).

	APL/S	APL	Definition
Scalar 2-argument functions	X+Y	X+Y	X plus Y
	X−Y	X−Y	X minus Y
	X×Y	X×Y	X times Y
	X÷Y	X÷Y	X divided by Y
	X*Y	X*Y	X to the Yth power
	X MAX Y	X⌈Y	maximum of X and Y
	X MIN Y	X⌊Y	minimum of X and Y
	X MOD Y		X modulo Y
		X|Y	X residue of Y
	X LOG Y	X⍟Y	base X log of Y
	X LT Y	X<Y	X less than Y
	X LE Y	X≤Y	X less than or equal to Y
	X EQ Y	X=Y	X equal to Y
	X GE Y	X≥Y	X greater than or equal to Y
	X GT Y	X>Y	X greater than Y
	X NE Y	X≠Y	X not equal to Y
	X AND Y	X∧Y	X and Y
	X OR Y	X∨Y	X or Y
Scalar 1-argument functions	+Y	+Y	Y
	−Y	−Y	negative of Y
	SIGN Y	×Y	signum of Y
	÷Y	÷Y	reciprocal of Y
	EXP Y	*Y	e to the Yth power
	CEIL Y	⌈Y	ceiling of Y
	FLOO Y	⌊Y	floor of Y
	ABS Y	|Y	absolute value of Y
	LOG Y	⍟Y	natural log of Y
	!Y	!Y	factorial of Y
	RAND Y	?Y	a random integer from 1 to Y
	NOT Y	~Y	not Y
Mixed 2-argument functions	X,Y	X,Y	the concatenation of X and Y, an array
Mixed 1-argument functions	SIZE Y	⍴ Y	number of elements in Y
	INDEX Y	⍳Y	1,2,. . .,Y
	ARRAY Y	Y ⍴ 0	size Y array of zeros
	,Y	,Y	Y ensured a vector
Subscripting	X(Y)	X[Y]	the element of X selected by Y
Assignment	X=Y	X←Y	X assumes the value of Y
Reduction operator	◎/Y	◎/Y	the ◎ reduction of Y, where ◎ is any scalar 2-argument function: Y_1◎Y_2◎. . .◎Y_n
Input	KEYB	⎕	keyboard input
Output	X	X	display the value of X
	"X"	'X'	display X
Circle functions	SIN X	1○X	sin X
(scalar 1-argument	COS X	2○X	cos X
functions in APL/S)	TAN X	3○X	tan X

Table 1: *APL/S functions with equivalent APL functions shown for comparison.*

Because of the limited character set available, the relational functions are denoted with alphabetic symbols (eg: NE for ≠) and assignment is denoted by = instead of the preferable ← of APL. In most other cases, functions which are denoted in APL by special characters are denoted in APL/S by the name of the function as given in descriptions of APL.

In APL/S, mathematical formulas are evaluated *left to right* with addition and subtraction done last. For example, 2*4+10×3−1 is evaluated as follows:

```
2*4+10×3−1
 16+10×3−1
  16+  30−1
       46−1
         45
```

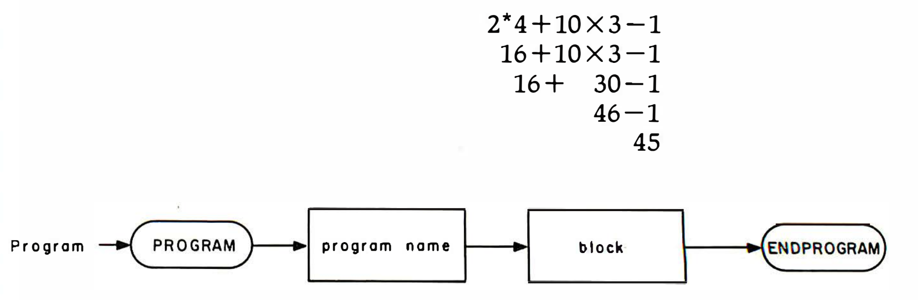
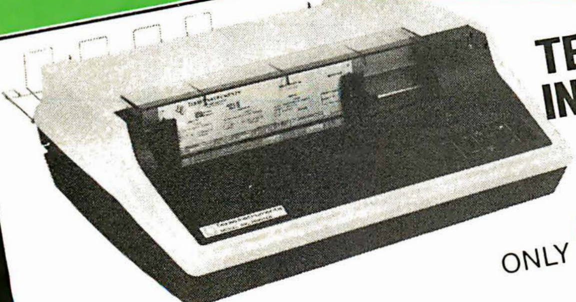


Figure 1: *Syntax diagram showing global structure of an APL/S program.*

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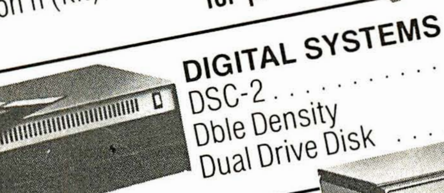
TERMINALS

LEAR-SIEGLER
ADM-3A....
ADM-31....
ADM-42....
} CALL* for prices

HAZELTINE
1400....
1410....
1500....
Mod 1 Edit....
} CALL* for prices

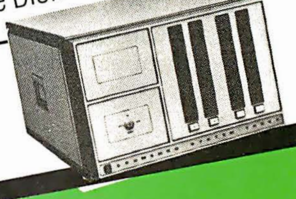
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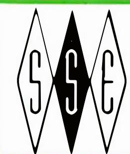
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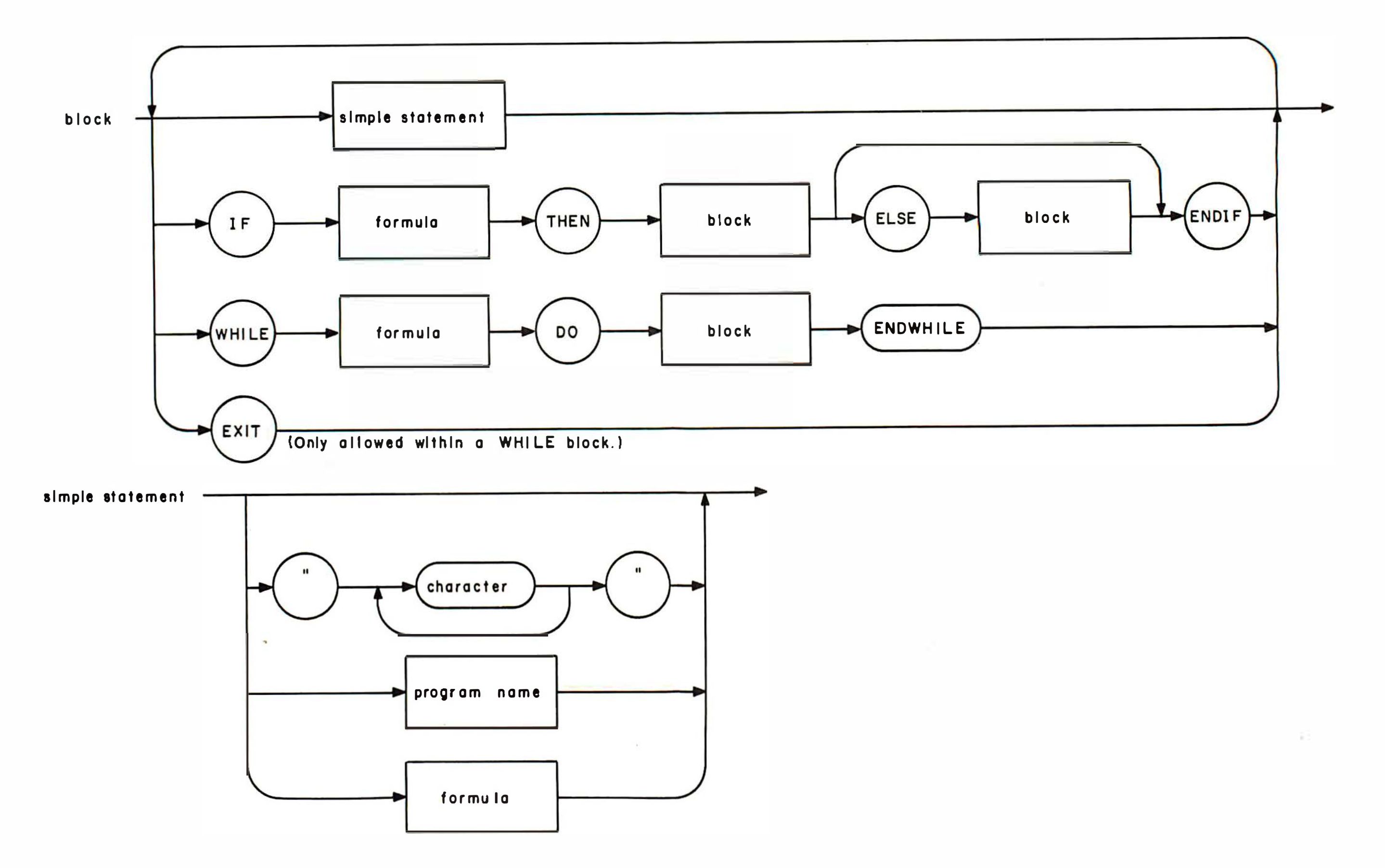


Figure 2: *Syntax diagram for block and simple statement structures.*

For an assignment statement, evaluation cannot be strictly left to right. For example, the statement A=10+1 is evaluated by first adding 10 and 1 for a result of 11, then assigning the 11 to A.

Evaluating the right hand side of an assignment before performing the assignment is carried forward to the case of an assignment embedded within a formula. For example:

```
3×A=10+1
3×A=11
3×11
33
```

The use of assignment within a formula is illustrated in the program GUESS of listing 1b in the line WHILE NUM NE GES=KEYB. The evaluation of the line goes as follows: the KEYB function reads the keyboard and returns the value entered, the assignment operation places the value into the variable GES, and the NE function is then evaluated to 1 if NUM is not equal to GES or to 0 if NUM is equal to GES. WHILE will then have an argument of 0 or 1.

WHILE, IF, AND, OR, and all the relational functions treat 1 as true and 0 as false. APL/S makes no data type distinctions such as boolean, integer, or real — a number is a number. Functions such as AND are defined on a subset of the numbers, namely 0 and 1.

The control figures of APL/S are Sequence; IF-THEN-ELSE, ENDIF; WHILE-DO, ENDWHILE; and Subprograms. There is no GOTO statement, but there is an EXIT for early termination of a WHILE loop. Because all control figures are self terminating (ie: ENDIF, ENDWHILE, ENDPROGRAM), there is no need for BEGIN-END pairs to form compound statements. Anywhere a single statement can appear, so can a block of statements.

Programs can be invoked recursively. The major weakness is that all variables are global. These facilities of the language are powerful enough that the popular eight-Queens problem can be solved by an APL/S program which closely follows the recursive and well structured solution given by Dijkstra. (The differences are array bounds and local variables.)

The eight-Queens problem was discussed from a beginner's viewpoint in an article in the October 1978 BYTE ("Solving the Eight-Queens Problem," by Terry Smith, page 122) and from a more sophisticated vantage by several readers in the February 1979 BYTE ("Eight-Queens Forum," pages 132 through 148). Dr E W Dijkstra's solution is found on pages 72 thru 82 of *Structured Programming*, by Dahl, Dijkstra, and Hoare (Academic Press, 1972).

Like APL, in APL/S all scalar functions are extended element-by-element to arrays, any scalar two-argument function can be used to reduce an array, and mixed functions such as SIZE (ρ in APL) are defined. Unlike APL, in APL/S arrays are restricted to one dimension, and subscript expressions must evaluate to scalars (or one-element arrays). Some examples should help clarify the array features.

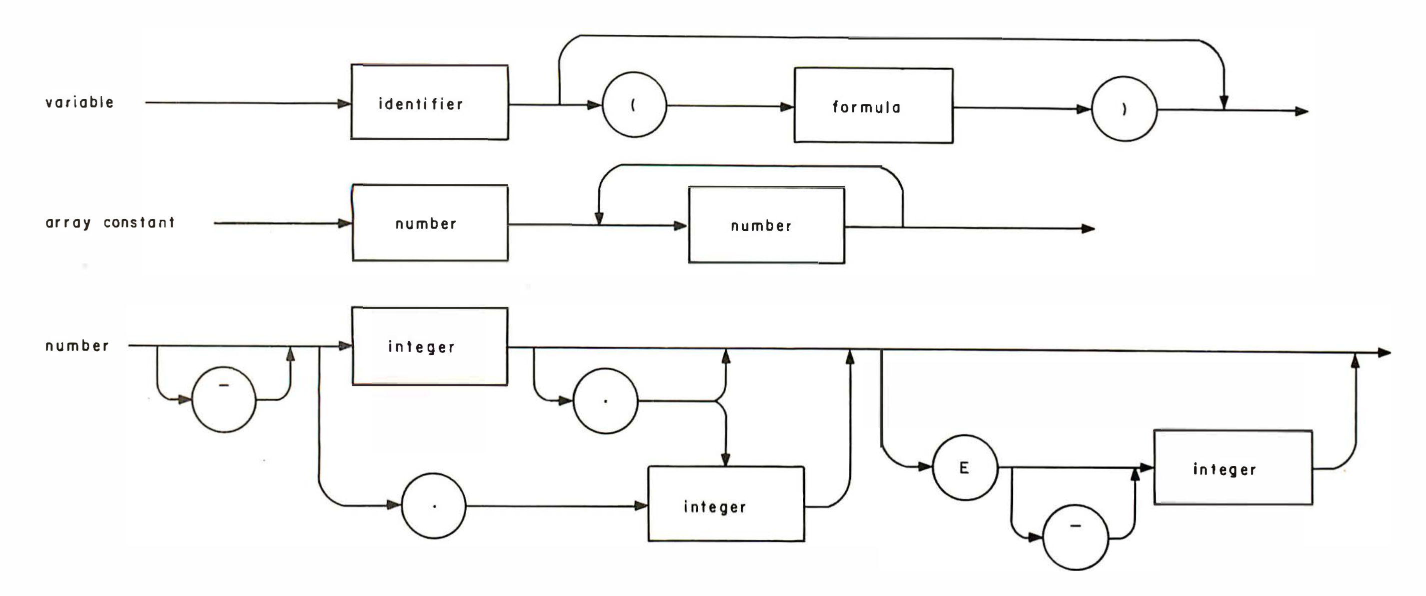


Figure 3: *Syntax diagram for variable, array constant, and number structures.*

Some Examples

Any *simple statement* (as defined in figure 2) can be entered for immediate evaluation. Photo 1 shows an example of an immediate mode calculation on the VideoBrain computer. The user entered +/2 4 6. It was evaluated and the result, 12, was displayed. The "2 4 6" is an example of an array constant. Addition was used to reduce the array to a scalar. Reduction by addition (+/) can be visualized as: +/2 4 6 gives 2+4+6 gives 12.

A more realistic use of arrays in immediate mode is the calculation of *net present value*. Given the one-dimensional array of cash flows, $C=(C_1,C_2,\ldots,C_n)$, the net present value (NPV) at an interest rate I, is given by:

$$NPV=\sum_{j=1}^{j=n}\frac{C_j}{(1+I)^j}$$

In APL/S, the formula for the net present value is:

+/(C÷((1+I)*INDEX SIZE C))

For comparison, the equivalent formula in APL is:

+/C÷(1+I)*ιρC

The two formulas are similar, differing only in function names and parentheses (to insure the same order of evaluation).

Because this kind of use of the array facilities is at the very heart of APL or APL/S programming, it is essential to understand how such formulas are evaluated. Let I=0.1 and C=¯100 50 150. The evaluation of the APL/S formula can be traced through its intermediate results:

```
+/(C÷((1+I)*INDEX SIZE C))
+/(¯100 50 150÷(1.1*INDEX SIZE ¯100 50 150))
+/(¯100 50 150÷(1.1*INDEX 3))
+/(¯100 50 150÷(1.1*1 2 3))
+/(¯100 50 150÷(1.1 1.21 1.331))
+/(¯90.909 41.32 112.7)
¯90.909+41.32+112.7
63.111
```

Text continued on page 98

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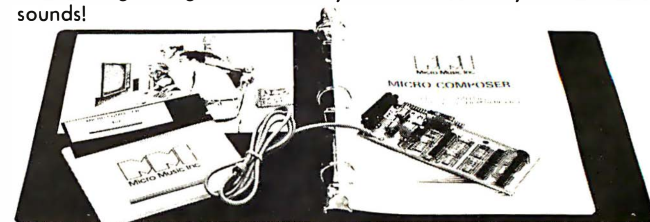
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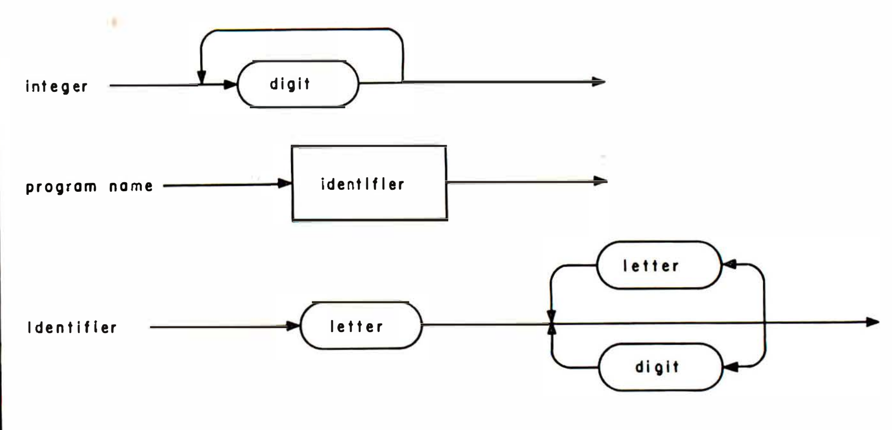


Figure 4: *Syntax diagram showing integer, program name, and identifier structures.*

formula
term
+
-
term

term
factor
factor
any 2-argument function except + or −

factor
KEYB
number
array constant
(
formula
)
variable
=
formula
any scaler 2-argument function
/
factor
any 1-argument function

Figure 5: *Syntax diagram of formula, term, and factor structures.*

Listing 3: *An APL/S program that simulates a game of craps. The game continues until a bet of $0 is made. Actual play is handled by the subroutine PLAY, which sets WIN to 1 to indicate a win, and to 0 for a loss. The net amount won is stored in NET.*

```
PROGRAM CRAPS
    NET=0
    "BET 0 TO QUIT"
    WHILE 1
    DO "PLACE YOUR BET"
        IF 0 GE BET=KEYB
        THEN EXIT
        ELSE "COMING OUT"
            PLAY
            IF WIN
            THEN "WINNER"
                NET=NET+BET
            ELSE "YOU LOSE"
                NET=NET-BET
            ENDIF
        ENDIF
    ENDWHILE
    IF NET GE 0
    THEN "YOU'VE WON"
        NET
    ELSE "YOU'VE LOST"
        -NET
    ENDIF
    "COME AGAIN SOON"
ENDPROGRAM
```

Listing 4: *The PLAY subroutine used by the CRAPS program of listing 3. A first roll of 7 or 11 wins; 2, 3, or 12 loses. Otherwise, a point is established (the value of the first roll). The dice are then repeatedly rolled until the point is rolled for a win, or a 7 is rolled for a loss. See listing 5 for a sample execution of CRAPS.*

```
PROGRAM PLAY
    +DICE=RANDOM 6 6
    PONT=+/DICE
    IF OR/(PONT EQ 7 11)
    THEN "PASS"
        WIN=1
    ELSE WIN=0
        IF OR/(PONT EQ 2 3 12)
        THEN "CRAPS"
        ELSE "YOUR POINT IS"
            PONT
            WHILE 1
            DO +DICE=RANDOM 6 6
                IF +/DICE EQ PONT
                THEN "POINT MADE"
                    WIN=1
                    EXIT
                ELSE
                    IF +/DICE EQ 7
                    THEN "BUSTED"
                        EXIT
                    ENDIF
                ENDIF
            ENDWHILE
        ENDIF
    ENDIF
ENDPROGRAM
```

Listing 5: *Sample execution of CRAPS.*

```
CRAPS
BET 0 TO QUIT
PLACE YOUR BET
?250
COMING OUT
4 3
PASS
WINNER
PLACE YOUR BET
?300
COMING OUT
1 1
CRAPS
YOU LOSE
PLACE YOUR BET
?200
COMING OUT
2 4
YOUR POINT IS
6
1 4
6 2
5 5
1 5
POINT MADE
WINNER
PLACE YOUR BET
?0
YOU'VE WON
150
COME AGAIN SOON
```

Text continued from page 94:

A simple program (AVE) using the array facilities is shown in photo 2 as it would appear to the user. The program computes the average of a set of observations. An execution of AVE is shown in photo 3.

The final example uses both the structured programming and array features for a simple game of craps. The main program is shown in listing 3, a subprogram in listing 4, and a sample execution in listing 5.

Both the main program and the subprogram use an EXIT statement to end a loop based on a condition detected inside the loop. The single entry, single exit convention of structured programming is maintained by this highly restricted type of GOTO.

The subprogram PLAY (listing 4) contains examples of using the array features for logical testing, a use which is not obvious in the numeric computation context usually employed in explaining the array features. Such nonmathematical use of the array features is common in APL programming, although in APL it is used in conjunction with a kind of conditional GOTO. The evaluation of the expression IF OR/(PONT EQ 7 11) will be followed through its intermediate results.

Although the purpose of the statement is logical testing, the execution trace will show how the statement is, in its use of the array features, similar to the expression for net present value. For tracing, let PONT=9.

```
IF OR/(PONT EQ 7 11)
IF OR/(9 EQ 7 11)
IF OR/(0 0)
IF 0 OR 0
IF 0
```

The result, 0, indicates that it is false that PONT equals 7 or 11, so execution will proceed to the first statement of the ELSE block.

Summary

APL/S is one of the first high-level language alternatives to BASIC to be offered on a low-priced personal computer (under $800). APL/S combines structured programming with an APL approach to arrays. Additional differences between APL and APL/S are due to hardware limitations and a desire to make use of the language as natural as possible. ■

An APL/S language system is available in a read-only memory cartridge for the VideoBrain home computer from VideoBrain Computer Co, 2950 Patrick Henry Dr, Santa Clara CA 95050.

REFERENCES

1. Brown, R G, "An Introduction to APL/S," *Conference Proceedings of the Third West Coast Computer Faire*, November 1978.
2. Dahl, Dijkstra, and Hoare, *Structured Programming*, Academic Press, 1972.
3. Judd, W and Cintz S, *APL/S User's Manual*, Video Brain Computer Co, Santa Clara CA, 1978.
4. Smith, Terry, "Solving the Eight-Queens Problem," October 1978 BYTE volume 3, number 10, page 122.

BYTE's Bits

Computer Simulates State Prison System, Helps Predict Cost

Louisiana State University (LSU) has designed several computer models that simulate the operation of the state's prison system. The computer models can determine the cost of building and staffing new prison units, the costs of prisoner transfer, and the costs that any changes in duration of stay or in legislation affecting probation or sentencing might have. With the University's IBM computer at their disposal, lawmakers can propose various pieces of legislation, send it to LSU for analysis, and receive a response within 48 hours. For further information, contact IBM, 7701 Stemmons Fwy, Dallas TX 75247.

Apple Computer Introduces a Repair Service

Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014, has announced a nationwide repair program featuring same-day computer repairs.

Level I repair requires no special technical knowledge and will be dealt with by a local dealer using new diagnostic software and Apple's Modular Parts Exchange Program (MPEP). The diagnostic program tests the motherboard, power supply, memories, keyboard, tape I/O, paddles, disk drive, and peripheral interface cards. When the problem is located, the diagnostic program identifies it and informs the dealer, through the video display, which component needs repair or replacement. The Level II (more complex) repairs will take place at a regional distributor, and Level III service will originate from the Apple Service Center in Cupertino CA.

A California School District Uses Computers

Five hundred and fifty boys and girls from elementary grades and the six high schools in the Huntington Beach school system are now using a powerful IBM System/370 Model 135, which is reserved exclusively for instructional purposes. The students take courses in mathematics, science, social studies, business, English, and computer programming languages in teacher-supervised classrooms on 56 terminals. A group of high school students wrote a series of online programs to carry all scoring and results of an academic decathlon hosted by a Huntington Beach high school. One student wrote a program to survey all county school professional salaries. Another 7th grade pupil won the county science fair with a computer project. Children can develop their own academic computing programs and make any program selection they want. For further information, contact Glen Dysinger, 5201 Bolsa Ave, Huntington Beach CA 92647.

LSU Professor and Computer Develop New Ways to Deal With Environmental Problems

An IBM 3033 processor and Richard C Farmer, professor of chemical engineering, are solving complex equations devised in the 1880s that describe the motions of solid particles in fluids. Computed results may show where to deposit sediment from dredging operations that are necessary

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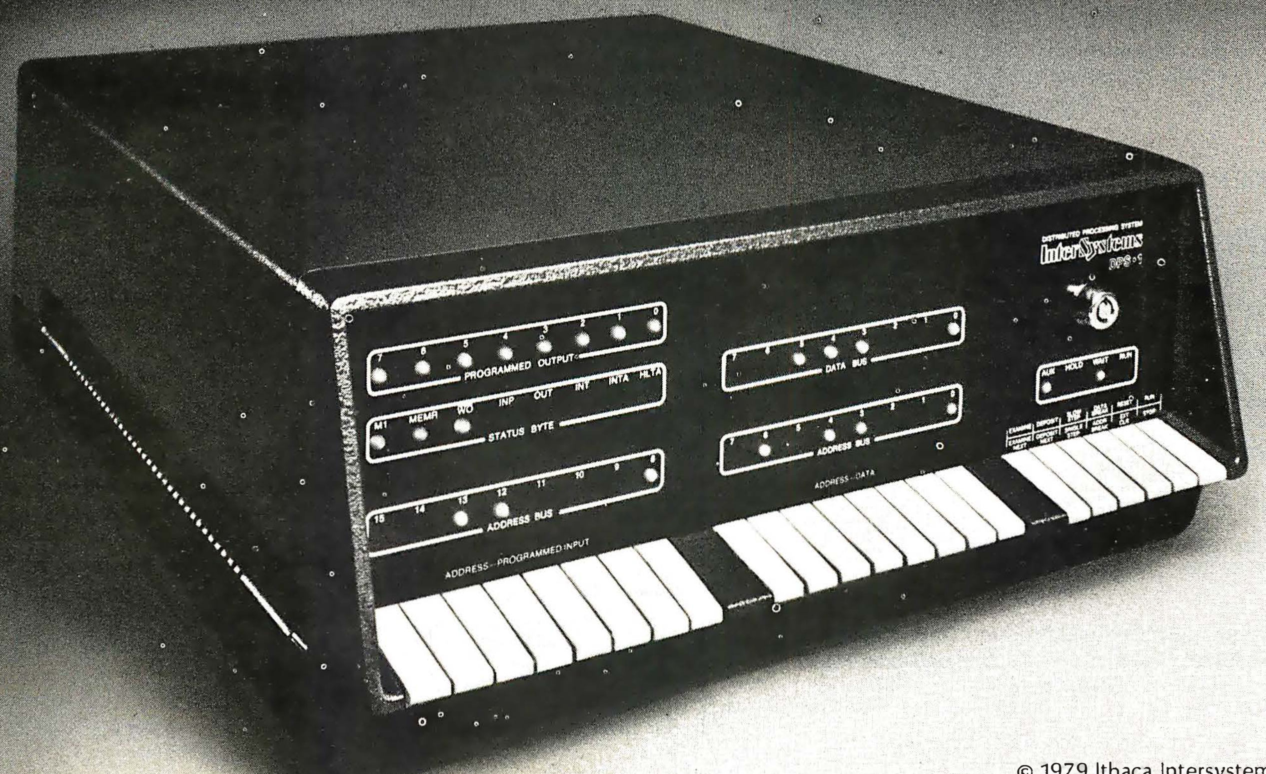
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to maintain shipping lanes, without endangering precious oyster beds. Professor Farmer hopes to find a way to halt the silting that blocks shipping, without creating other environmental problems. Before a computer approach was developed, marine scientists had to depend on photos and dyed water, and civil engineers used scale models to study environmental problems. The Tennessee Valley Authority uses Professor Farmer's approach to determine optimum methods, from an environmental standpoint, to dispose of the waste heat from power plants. The Louisiana State University, Office of Information Services, Baton Rouge LA 70803 has more information on computer-assisted programs in environmental studies.

Short Course Series

Integrated Computer Systems Inc, 3304 Pico Blvd, POB 5339, Santa Monica CA 90405, has announced their winter and spring schedule for their Short Course series. Courses on computer graphics, digital signal processing, troubleshooting microprocessor systems, and other topics will be covered. The courses are being held in major cities around the US. These courses are structured for technical and managerial personnel.

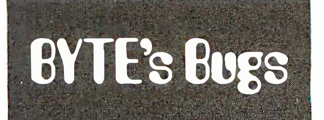
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Call for Papers

The Instrument Society of America (ISA) is sponsoring a conference on the theory, design, manufacture and use of instrumentation, computers and systems for measurement and control entitled "Instrumentation of Challenge," to be held October 20-23, 1980, in Houston. Papers concerning theory, applications, technique or innovations in the fields of aerospace, analysis, cryogenics, data handling and computation, metals, power, textiles, pulp and paper, maintenance, biomedical, and more, are welcome.

To submit a paper for consideration, request abstract forms from ISA headquarters, 400 Stanwix St, Pittsburgh PA 15222. Deadline for unsolicited papers is February 1 1980. ■



Some Refreshing Bugs

Thanks go to Steve Ciarcia for uncovering several bugs in his October 1979 BYTE Circuit Cellar article, "Self-Refreshing LED Graphics Display." In figures 2 (page 59) and 4 (page 62) the light-emitting diodes (LEDs) are shown with their polarities reversed. For proper operation, they should be reversed from their appearance in the figures. Also, in figure 2 the signal decode I/O write strobe is shown as a high-to-low transition. It should be a low-to-high transition for proper operation. ■

BYTE News . . . .

FCC TO ALLOW ASCII COMMUNICATION VIA OSCAR: The Federal Communications Commission (FCC) has granted the American Radio Relay League (ARRL), the largest amateur radio association in the world, a waiver to allow ASCII communications via the OSCAR satellite. Radio amateurs who have personal computers will soon be able to transmit and receive ASCII anywhere in the world. The waiver covers "experimental use only," as there are still some problems. The problems involve radio frequency (RF) interference in the satellite receiver and a lack of a clear-cut protocol for the ASCII format. Progress is being made in solving these problems, and it is expected that amateurs will utilize this service heavily.

UNIX-LIKE SYSTEM AVAILABLE FOR 8080/Z80 SYSTEMS: An operating system modeled after UNIX (registered trademark of Bell Labs) is now available from the Computer Systems Design Group, 3632 Governor Dr, San Diego CA 92122. UNIX is a high-level, timeshare operating system developed by Bell Labs to run on large DEC PDP-11 systems. It has proven very popular at educational institutions, research organizations, and the like, because of its power and flexibility.

COMPUTER BULLETIN BOARDS MULTIPLY: Computerized bulletin board systems are multiplying like rabbits! These systems, which allow people to communicate with others via terminal/modems and personal computer systems, are skyrocketing in popularity. From only three computerized bulletin board systems in operation at this time last year, their number has increased to nearly 60 systems in operation across the country. These systems are run by individuals, clubs and businesses who are using the computerized bulletin board systems' software to set up computerized intelligent answering machines. Many are tailored to the special needs of the sponsors by altering the software. California has nearly twenty computerized bulletin board systems in operation and Texas approximately ten. A majority of the computerized bulletin board systems can be contacted via computer club newsletters.

NEWS BRIEFS: Bell Labs, Murray Hill NJ, has fabricated experimental bubble memory chips with 11.5 M bit density to yield working storage of at least 1 M bytes . . . . Bell Labs has also announced an extension of the conventional doping methods used in manufacturing integrated circuits that could double their speed . . . . National Semiconductor, Santa Clara CA, has announced a CMOS microprocessor which executes the Z80 instruction set. However, it is not pin-compatible with the Z80 . . . . Texas Instruments is the leader in microprocessor production. So far they have made over 9 million TMS-1000 microprocessors. The TMS-1000 is a 4-bit processor used mostly in toys and games.

8-INCH HARD DISK DRIVE MARKET SHAPING UP: It is now apparent that manufacturers are going to use the new 8-inch hard disk drives in a big way next year. The 8-inch hard disk drives will fill a gap that exists between floppy drives and the 14-inch hard disk drives. The IMI-7710, made by International Memories Inc, Cupertino CA, is the only drive currently in production. IMI appears to have at least a 6-month, and possibly greater, lead on the rest of the manufacturers. The 7710 stores 11 M bytes and sells for under $2000 in quantity ($2990 for a single unit).

At least a dozen manufacturers will have 8-inch hard drives in production by the end of the first quarter of next year. They will range from 2.1 M bytes all the way up to 51 M byte units, with prices ranging from $1900 to $4000 in single-unit quantities. Shugart will be a late entry into this market and is keeping development efforts under wraps. However, Shugart is expected to introduce a very low-cost small storage size drive.

It is expected that manufacturers of double-sided floppy drives will have all the bugs solved in 1980 and that these drives will hinder the low-end, 8-inch hard disk drive market. On the high-end, the 14-inch hard disk drives, although physically larger, have a lower cost per bit and hence may limit the growth of 8-inch drives. It is expected that the more popular 8-inch hard disk drives will be in the 5 to 20 M byte range.

RANDOM RUMORS: General Electric is interested in the personal computing area. They have invested some money in Intelligent System Corp (ISC), the maker of Compucolor systems. But they have not decided on their approach . . . . Shugart is producing 1000 5-inch floppy disk drives per day, while Micropolis, ranked second in the industry, is turning out 200 per day . . . . A 2 M byte

5-inch floppy disk drive will be announced this coming spring by Tandon Magnetics, Chatsworth CA. The drive will be double-sided and double-density with 96 tracks per inch and 12,000 bits per inch.

16-BIT MULTIPROCESSOR UNIT PERIPHERAL INTEGRATED CIRCUITS BEING INTRODUCED: All of the 16-bit microprocessor manufacturers are introducing peripheral integrated circuits which increase the power and flexibility of the new 16-bit microcomputer systems. These integrated circuits will allow these microcomputers to take over applications once considered the province of mini or large computer systems. These include memory management (MMU), bus arbitration, direct memory access (DMA), and floating point arithmetic. Also being introduced for the 16-bit devices are dual-density floppy disk, bubble memory, and super fast printer controllers.

The memory management unit allows the microprocessor to partition off its own memory space. Motorola and Zilog plan to have memory management unit integrated circuits for their 68000 and Z8000 multiprocessor units, while Intel includes the memory management unit with their 8086 16-bit multiprocessor unit.

Bus arbitration controllers are used in multiprocessor systems where there is more than one master unit on the bus. The bus arbiter provides the necessary timing and control signals, including establishing priorities among masters. Intel has already announced such an integrated circuit and Motorola and Zilog are designing theirs.

AMD has released its arithmetic processor which performs single-precision (32-bit) and double-precision (64-bit) add, subtract, multiply, and divide operations with 16-bit wide data paths.

WHAT'S AHEAD FOR 1980?: This is a good time to make some predictions for next year. What can we expect? Let me stick my neck out a little. I expect to see the following:

- The first Japanese personal computer systems will become available in this country.
- Competitive pressures will increase on small manufacturers. This will cause some liquidations and several mergers, consolidations or acquisitions.
- A sizable number of audio and office equipment retailers will enter the computer retailing business. This will create pressures on conventional computer stores. We may even see the appearance of stores that sell only software, much like audio record stores.
- 16-bit microcomputer systems will be commonplace. They will have multiuser, multitasking and multiprocessing, and greater real-time operating capabilities. They will offer far more sophisticated editors, debuggers, compilers, assemblers, and other system software.
- IBM, Digital Equipment Corp, Data General, Hewlett-Packard and other minicomputer makers will introduce low-cost microcomputer systems to compete with current microcomputer systems.
- Several personal computer manufacturers will introduce "second generation" machines with significant increases in power.
- The emphasis will shift from hardware to software. BASIC will continue as the dominant language. Enhancements will continue to be made to the available BASIC interpreters. BASIC compilers will be more available. Pascal will increase in popularity, but will still be used by only a small percentage of system programmers. New COBOL compilers will also become available and increase in popularity. APL will also increase in popularity, particularly for financial and statistical applications. Also a large number of data base managers will be introduced.
- Business application software for microcomputer systems will finally "come of age" and provide the needed performance that suppliers have been promising but not delivering during the past two years.
- The first low-cost microcomputer-based robot kit will be introduced.
- Typewriters will have built-in intelligence, using microprocessors and built-in microdisks naturally, and will have many word processing features. They will be able to store 10 to 50 pages of text. The "dumb" typewriter will soon be a thing of the past.
- Personal computer time-sharing systems will proliferate. The greatest use will be for accessing data bases.

MAIL: I receive a large number of letters each month as a result of this column. If you wish a response, please include a stamped, self-addressed envelope.

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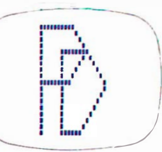
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Text Compression

James L Peterson
Dept of Computer Sciences
University of Texas
Austin TX 78712

A continuing problem on any computer system is storage. There is never enough computer memory for all the information we wish to store. This is true both for programs in main memory and for the information which resides on peripheral devices.

One solution to this problem is simply to buy more memory. Particularly in the case of storage devices with removable media such as cassettes, floppy disks, magnetic tape and even paper tape, additional media can be purchased and used as necessary. But even here economics will eventually limit the amount of storage available.

An alternative approach is to try to make better use of existing storage media. This is where *text compression* can be of great use. The idea of text compression is to reduce the amount of space needed to store a file by compressing it, making it smaller. Compression is accomplished by changing the way in which the file is represented. The *encoding* procedure is performed in such a way that it is reversible; that is, it can later be *decoded* to produce the original uncompressed file. This is illustrated in figure 1. The hope is that the encoded version of the file will be smaller than the original file, and hence space will be saved.

The cost of this space saving is processor time. Additional processor time will be needed to encode and decode the compressed files as they are processed. However, it should be noted that microprocessors are seldom processor bound, but more commonly have extra processor cycles available. In fact, the total execute time of many programs will be less on a compressed file despite its encoded form. This is because the I/O(input/output) transfer time for a compressed file is less than the transfer time for an uncompressed file, since there are fewer bits to read or write. Hence, I/O bound programs (like assemblers and loaders) may execute faster on compressed files.

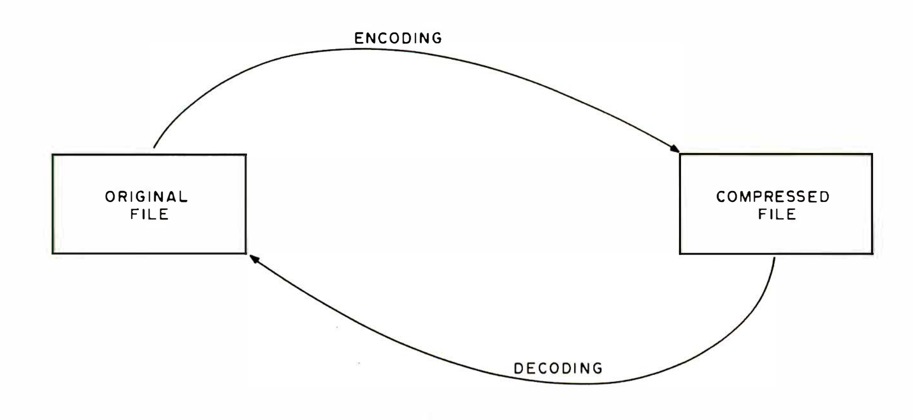


Figure 1: *The text compression process.*

The basic idea of text compression is to find an encoding method that takes up minimal space. Many algorithms for text compression have been invented, and we present some of them here. In general, these algorithms will work for any type of data, such as numeric, character string, and so on; but for purposes of this article we limit ourselves to text, ie: strings of characters. This will include programs, documentation, mailing lists, data, and many other files stored in computers. In fact, object programs, if considered as simply strings of bytes, can also be compressed, although this must be done carefully.

Text compression is accomplished by careful selection of the *representation* of the information in the compressed file. For many small computer systems, the ASCII code is generally used to represent characters. The main advantage of the ASCII code is that the representation is standard and easy to define. A major disadvantage is its poor space utilization. ASCII is a 7-bit code, while most processors handle 8-bit bytes. Thus, 1 bit out of 8 (12.5%) is wasted simply because a 7-bit character code is used in an 8-bit byte. Further, most control codes are seldom used, and many applications do not need both upper and lower case characters. Thus, another bit can generally be reclaimed with ease, providing at least 25% savings in storage space. Many of the algorithms presented here can turn these extra bits into even greater savings of space.

Notice, however, that this approach requires a description of how the compressed file is to be represented. This description commonly consists of the encoding and decoding routines. The savings which result from text compression must be balanced against both the additional processor time for encoding and decoding, and the storage space necessary for the encoding and decoding routines. Also, different types of files may be best encoded by different methods, so several different encoding and decoding routines may be necessary.

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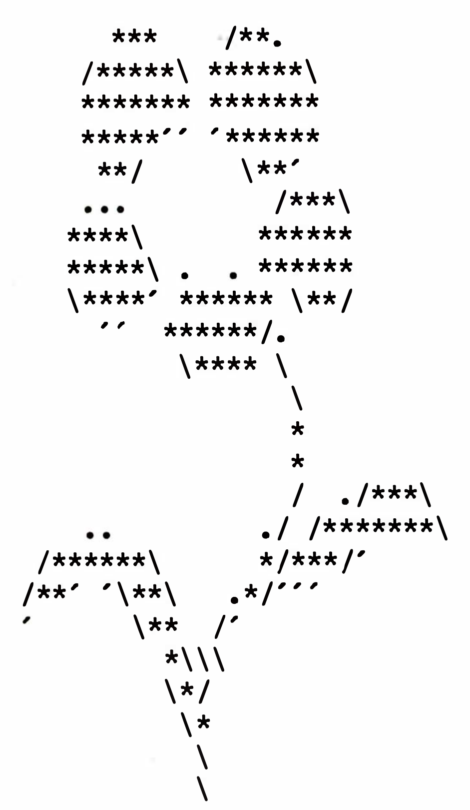


Figure 2: *A file which can benefit from simple text compression techniques. The original file is a 24 by 80 character video display image consisting of 1920 characters. Deleting trailing blanks and using tabs set for every 8 columns will reduce the size of this file to 412 characters — a savings of 78.6 percent.*

```
$32 $3*$4 /**.@$30 /$5* \  $6* \ @$30 $7*  $7*@$30 $5*'' '$6*@$31 **/$6  \ **'@$30
$3.$9  /$3* \ @$29  $4* \ $7  $6*@$29  $5* \ .    .  $6*@$29   \ $4*'  $6*    \ **/@$31  ''
$6*/.@$36  \ $4*   \ @$43   \ @$43  *@$43  *@$43 /    ./$3* \ @$30  ..$9  ./ /$7* \ @$27
/$6* \ $6*/$3*/'@$26/**'  ' \ ** \ $3.*/$3'@$26'$6 \ **/'@$35*$3 \ @$35 \ */@$36 \
*@$37 \ @$37 \ @
```

Figure 3: *Further compression of the file shown in figure 2 done by replacing multiple identical characters with an escape sequence. The escape sequence in this case is the escape character $ followed by the number of repetitions and the character to be repeated. This scheme is useful only when the repeat count is greater than 2. The count would normally fit into 1 byte, but is here shown in decimal. The character @ represents the carriage return and line feed. Only 287 characters are needed to represent the file in figure 2 using this representation. This reduces the file to 14.9 percent of its original size.*

Trailing Blanks and Tabs

A simple approach to compression for text files (but not for object code files) is eliminating blanks which come at the ends of lines before the carriage return and line feed characters. These are known as trailing blanks. For systems which store large amounts of assembly language, BASIC or FORTRAN programs, much of each line will be blank. Any trailing blanks can be deleted without changing the meaning of the file.

Tabs can be used to reduce the number of blanks elsewhere in a line. Particularly with block structured programs, such as ALGOL, Pascal, or PL/I, or with column oriented languages such as FORTRAN or assembly language, tabs can be quite effective in text compression. Two varieties of tabbing mechanisms can be used. One is called *fixed tab stops.* In this case, tab stops occur every **n** columns, where **n** is a system-wide constant. Typically **n**=8, although some studies have shown that **n**=4 or **n**=5 will produce additional savings.

The other possibility is to use *variable tab stops.* In this case, tab stop positions are selected for each file separately. This would require a decision as to which tab stops are best (ie: which would produce the best compression). In addition it would be necessary to indicate with each file what tab settings are to be used. This can be done easily by appending a tab stop dictionary at the head of each file. Such a dictionary would be used to initialize tables for the decoding routine which would replace each tab with an appropriate number of blanks. This approach allows different tab settings to be used for different programming languages or data sets.

Multiple Characters

Trailing blanks and tab mechanisms are used for compressing strings of multiple blank characters. Some applications may result in strings of identical nonblank characters occurring frequently. For example, picture processing by computer often requires storing long sequences of identical characters, such as the characters which produce figure 2. The approach here is to replace a string of **n** identical characters by the number **n** and 1 character, thus saving **n**-2 characters. The count can be represented as a byte. If the count exceeds 256, it can be output as a count of 256 followed by the character, and then another count and character for the remainder.

Encoding consists of simply counting identical characters until a different one is found, and then outputting the count and character. Decoding simply expands each count and character to the appropriate number of characters.

Obviously, **n** should be greater than 2 most of the time for this approach to succeed. If **n** were generally 1, this approach would actually double the size of the file. Since this is commonly the case for text files, a more sophisticated approach is generally used.

We wish to replace sequences of identical characters by a count and character, but leave single or double characters alone. The problem is representing the multiple characters in such a way that the count is not misinterpreted as a character. A common solution is to use an *escape* sequence, which is a means of indicating that a special interpretation should be applied to the characters which follow. To create an escape sequence, choose any character which is seldom (preferably never) used. For example, in ASCII one of the control codes or special characters might be used. ASCII even provides an escape character, but if it is already being used for another purpose, any other character code can be used. Now a sequence of n identical characters would be represented by the escape character, the value **n**, and the character to be repeated. Figure 3 shows the text of figure 2 compressed by this method.

This allows normal text to be represented normally, except for the escape character. The problem we must now solve is how to represent the escape character if it occurs in the input (uncompressed) text. If we simply copy it to the compressed file, the decoder will (incorrectly) think it is the start of an escape sequence and interpret the following 2 characters as indicating a sequence of identical characters (this is essentially the same problem that language designers face in trying to represent a quoted string consisting of a quote). Several approaches to this problem can be used: outlaw all occurrences of the escape character; replace all escape char-

```
 10 READ A                      10 $5 A
 20 IF A=0 THEN 110             20 $2 A=0 $6 110
 30 IF A>0 THEN 80              30 $2 A>0 $6 80
 40 LET B=-A                    40 $3 B=-A
 50 LET R=SQR(B)                50 $3 R=SQR(B)
 60 PRINT A,R," $ "             60 $4 A,R," $$ "
 70 GO TO 10                    70 $1 10
 80 LET R=SQR(A)                80 $3 R=SQR(A)
 90 PRINT A,R                   90 $4 A,R
100 GO TO 10                   100 $1 10
110 END                        110 $7
```

Figure 4: *Compressing a BASIC program by using keyword replacement. The keywords (1) GO TO, (2) IF, (3) LET, (4) PRINT, (5) READ, (6) THEN and (7) END have been replaced by an escape sequence consisting of an escape character $ followed by a keyword number. Note that the escape character occurred within the original program and was replaced by a special escape sequence $$. In actual use, all delimiting blanks around keywords would be subsumed into the keyword. Thus line 10 would be 10$5A, and $5 would mean "READ".*

acters by a special escape sequence such as one with a 0 count; replace all escape characters by an escape character, a count of 1, and an escape character, treating it as a sequence of length 1. Any of these approaches will allow a file to be encoded and decoded easily and correctly.

Note that, in choosing an escape character, we can always use the same one (a system-wide constant) or we can select a different one for every file. If we choose a different one for every file, we must make a preliminary pass through the file to look at all characters used and find one which is not used. We should then append the escape character at the beginning of the file to allow the decoding algorithm to know what character is used as the escape character.

Keyword Replacement

A very common type of file stored in computer systems is a program file. Programs offer great possibilities for text compression because of their stylized form and syntax. The techniques of deleting trailing blanks and using tabs to replace leading blanks can reduce storage requirements considerably. But an even larger gain can be made from keyword replacement.

Most programming languages use a number of *keywords* or *reserved words*: in FORTRAN, such words as INTEGER, FORMAT, CALL and so on; in BASIC, such words as LET, READ, PRINT, REM and so on. These words are used throughout these programs and are prime candidates for text compression.

Two techniques are commonly used. First, one can replace each keyword by an escape sequence. The escape sequence might consist of the escape code, followed by a number which indicates which keyword is being used. This has the advantage of allowing a large number of reserved words up to the number which can be held in 1 byte, and can be particularly useful for assembly language symbolic op codes.

An alternative approach is to look through the existing character code for unused character codes. For example, if ASCII is being used, many of the control codes, some of the special characters, and perhaps the lower case characters are not normally used. If 7-bit ASCII is being used with 8-bit bytes, then the extra bit can be used to define 128 new unused codes. These unused codes are paired up with the most frequently occurring reserved words. One code should be reserved for use as an escape or quote character, in case any of the codes assumed to be unused should happen to be used in an input file.

For encoding, the input file is scanned for reserved words and each reserved word is replaced by the appropriate special code as illustrated by figure 4. If any of the special codes should show up in the input stream, they are replaced by the 2-character sequence of the escape code followed by the input character. For decoding, all special codes are replaced by their equivalent keyword, except that any character preceded by an escape code is copied directly to the output, with no replacement.

At this point, a problem may become apparent. Note that the keywords for any particular language are fixed and relatively small in number, but that the keywords vary from language to language. Hence, the appropriate correspondence between special codes and reserved words may vary greatly. In single language systems (such as those which offer only BASIC) this is not a problem, but more general systems need to consider this problem.


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...olutions are available. ...an simply use separate en... ...and decoding routines for ...nguage, leaving it to the pro... ...mer to use the appropriate one. ...cond, one can tag each compressed ...ile with a byte which indicates if this is a BASIC compressed file, or a FORTRAN compressed file, or a type X compressed file. Then the encoder must either be told how to encode the file or be able to guess (or compute) that it is a FORTRAN, BASIC, or type X file and apply the appropriate compression algorithm. The compressed file is tagged as it is encoded. The decoder looks at the tag and uses the appropriate decoding scheme.

A third approach is more general, but potentially more expensive. The difference between the encoding and decoding algorithms for the different types of files is simply the table of pairings between keywords and character codes. Therefore, another approach is to prefix each compressed file with a dictionary of character code and reserved word pairs. The dictionary explains the meanings of the special character codes by indicating the reserved words for which they stand.

```
Dictionary:     $A "the"
                $B "text compression"
                $C "computer"
                 ...

Text:
    This paper is concerned with $A use of $B in $C systems, where $A amount of $C storage is
    limited.
    ...
```

Figure 5: *Text compression by substring replacement. Substrings are replaced by abbreviation codes (here we use escape sequences). A dictionary is placed at the beginning of the file to define the meanings of the abbreviations.*

Substring Abbreviation

The idea of appending an abbreviation dictionary to the front of a compressed file opens the way to using the keyword replacement scheme for more general files. The idea is quite simple. Pick out those sequences of characters which occur most frequently in a file and replace them with a special character code. To allow decoding, we append a dictionary at the beginning of each file to show which special character codes correspond to which replaced character strings. This approach can yield very good text compression, especially for programs or natural language text, since keywords, variable names and some words (like *the*, *and*, and so on) are used very frequently.

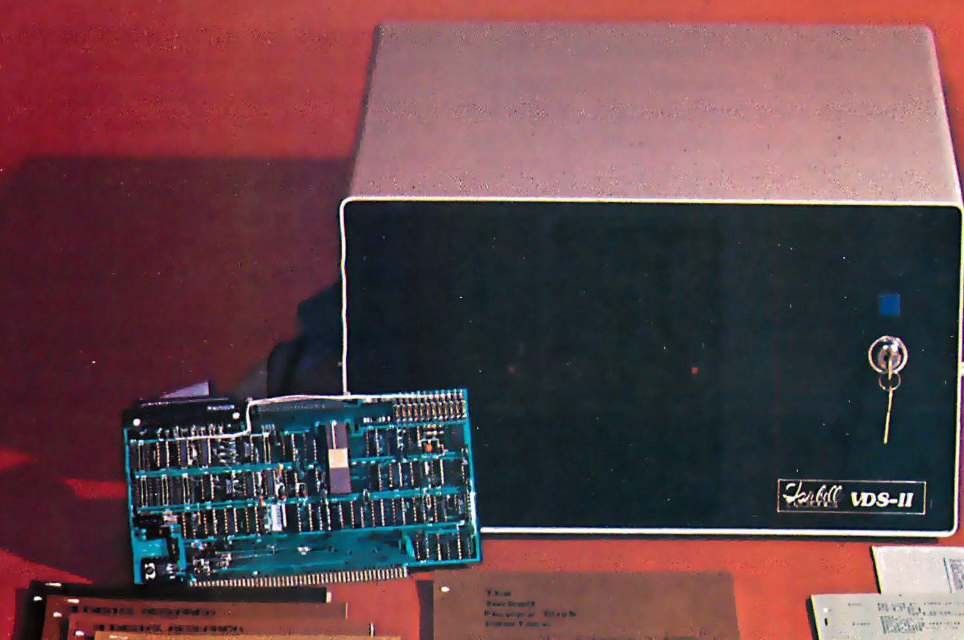
But there are some problems with this approach also. The major problem is selecting the character strings to be abbreviated. With programs written in particular languages, keywords occur frequently and so are a safe bet for substitution, but what constitutes appropriate character strings for general replacement? These can be determined only by examining the file, since the appropriate strings will vary from file to file.

The objective, of course, is to realize the greatest savings in space. Here we are limited mainly by the number of codes available for substitution. If we use unused codes in the existing character set, we are limited to from 10 to 50 abbreviation codes, typically. If we extend the character set (say by using 8-bit codes with 7-bit ASCII) then we may have as many as 128 codes available. Using an escape sequence may provide up to 256, but at a cost of at least 2 characters per abbreviation. In all cases, the number of codes available will always be limited to, say, **m**. Thus we need to pick those **m** strings for abbreviation which will result in the greatest space savings.

We do not always want to pick merely the most frequently occurring **m** strings. Consider the 2 strings *to* and *text compression*. If *to* occurs 100 times and *text compression* only 15 times, which should we replace? Replacing the 2-character sequence *to* by a single abbreviation code saves only 1 character (assuming 1 byte abbreviation code) per occurrence, or a total of 100 characters. Replacing the 16-character sequence *text compression* saves 15 characters per occurrence, or 225 characters total. Thus, in general we wish to replace that character sequence whose product of length and frequency is greatest. An example of substring replacement is shown in figure 5.

The encoding problem then becomes that of finding the **m** sequences whose length-frequency product is greatest, replacing all occurrences of them with the **m** abbreviation codes, and appending the abbreviation dictionary at the front of the compressed file. The decoding problem reduces to

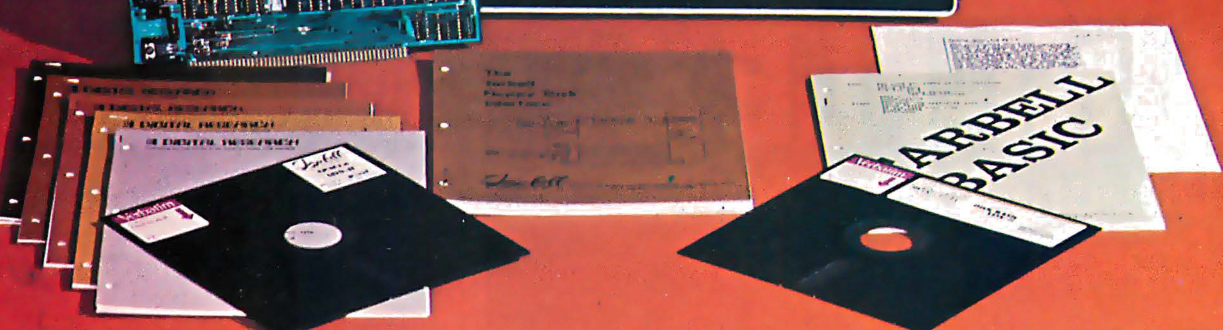
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merely reading in the abbreviation dictionary and replacing all abbreviation codes with the appropriate character sequence.

The only real difficulty is finding the **m** sequences to be abbreviated. No really good solution to this problem is known. The best solution I have seen works as follows: first, make 1 pass through the file to compute the most frequently occurring pairs. There should be no more than 2500 of these, and probably many fewer. Compute the frequency of these pairs and keep only the **m** or **2m** most frequent. Now consider that any sequence of length 3 both begins and ends with a subsequence of length 2, and that these 2 subsequences of length 2 must be at least as frequent as the length 3 sequence. That is, if there are 23 occurrences of *abc*, then there must be at least 23 *ab* and at least 23 *bc*. Thus we can make another pass through the file, counting the frequency of subsequences of length 3, but limiting ourselves to those sequences which begin and end with subsequences of length 2 (which are also frequent). Next we can make another pass for length 4 (limiting the sequences to those with frequent length 3 subsequences), another pass for length 5, and so on until we decide to stop. We can stop either when our last pass has produced no new sequences whose frequency-length product exceeds the previous set, or after a fixed number of passes.

Huffman Coding

All of the schemes for text compression discussed so far are similar in the sense that they confine themselves to working within the given character code and byte structure. Even more savings can result from recoding the character code representation itself. Almost all character code representations use a fixed code size: 6 bits for binary coded decimal(BCD), 7 bits for ASCII and 8 bits for EBCDIC. This can be very wasteful of space.

Consider the simple problem of encoding the 4 characters *A, B, C,* and *D*. If we use a fixed code size, then we could encode each character with 2 bits, as follows:

A 00
B 01
C 10
D 11

But suppose that the letter *A* occurs 50% of the time in the text, *B* occurs 25% and *C* and *D* split the remaining 25% equally. Then the following *variable* length character code will produce a shorter *average* text length.

A 0
B 10
C 110
D 111

To compute the average text length, consider that, out of **n** characters, **n/2** will be *A* which requires only 1 bit, **n/4** will be *B* for 2 bits each and the remaining **n/4** will be *C* or *D* for 3 bits each. Thus the total number of bits to represent **n** characters is:

$$1(n/2) + 2\,(n/4) + 3\,(n/4) = 1.75n$$

Comparing this with the **2n** bits needed for the fixed length code, we see that we have saved 12.5% of the total file size.

Variable length coding and decoding is somewhat more complex than fixed length coding, but not really difficult. It involves much more bit manipulation. To encode a string like *ABAABCDAB*, we simply concatenate the bit representations of each character, packing across byte boundaries as necessary.

A	B	A	A	B	C	D	A	B
0	10	0	0	10	110	111	0	10

To decode, we must scan from left to right, looking at each bit. For the string 01001100, we notice that the 1st bit is a 0. Only *A* starts with 0, so our 1st character is an *A*. The next bit is a 1, so it could be a *B, C* or *D*, but looking at the next bit we see that the next character must be a *B*. We remove the 2 bits for the *B*, and continue. The next bit is 0, so the next character is an *A*. The following bit is a 1, signifying either a *B, C,* or *D*. The next bit is a 1, signifying a *C* or *D*. Finally the next bit indicates a *C*. The last character is an *A*. So our decoded text is *ABACA*.

Computer stored text files can benefit greatly from Huffman coding. Huffman coding can be used anytime

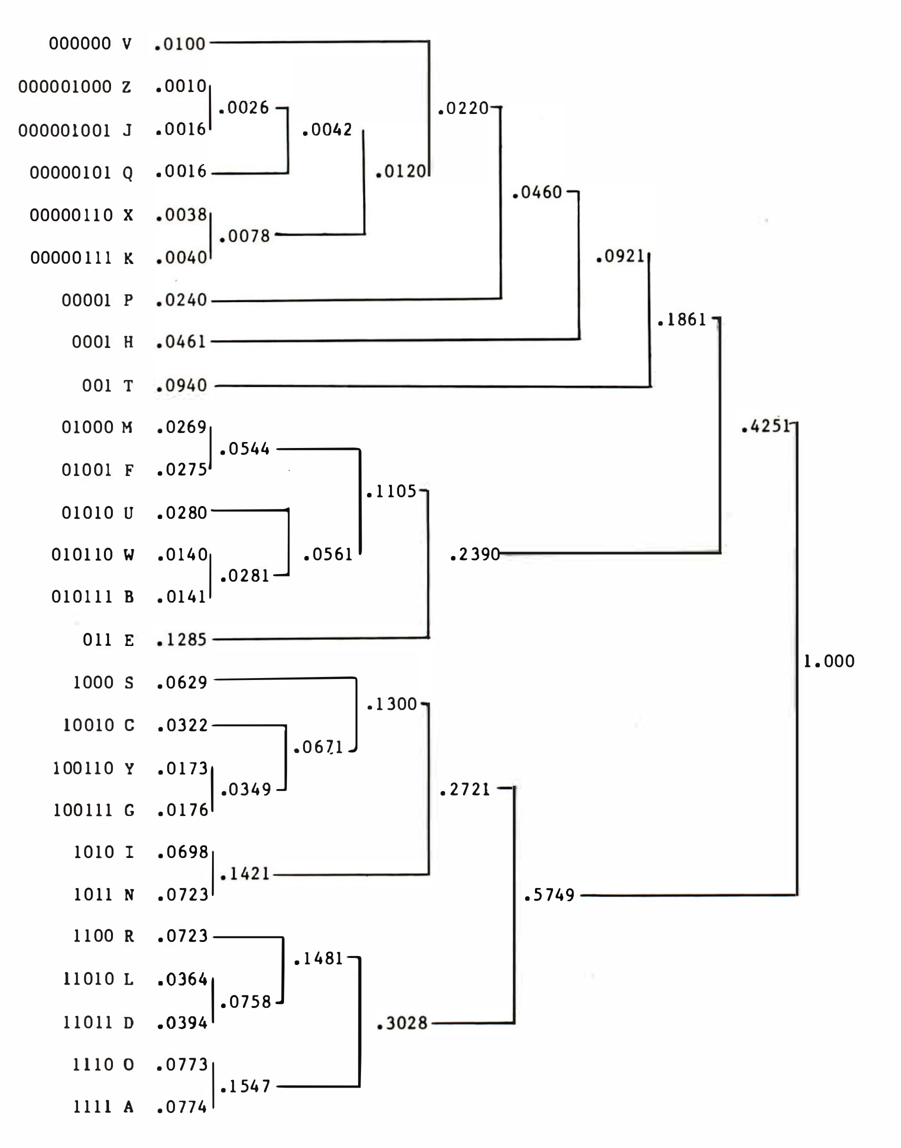


Figure 6: *Huffman code for the letters of the English language, based on the probabilities (frequency of occurrence) of the letters in English. The code length is inversely proportional to the frequency of occurrence of a given letter (in much the same manner as Morse code). Code lengths vary from 9 bits (for z and j) to 3 bits (for e and t). The average length is 4.1885 bits per letter. Five bits would be necessary for a fixed length code, a space saving of 16 percent.*

the probabilities of the character codes are not equal. In fact, the more unequal the probabilities, the better the compression with a Huffman coding. Looking at a table of frequencies of the letters in English, we can see that they are quite unequal, and hence can be compressed nicely with Huffman coding.

To construct a Huffman code, a very simple algorithm is used (refer to figure 6). First, it is necessary to compute the probabilities of the characters to be encoded. This requires 1 pass through some sample text, a part of a file, the whole file or several files, as desired, counting the occurrences of different characters. Then we need to sort the characters according to their frequency. Take the 2 least frequently occurring characters, and combine them into a *super character* whose frequency is the sum of the 2 individual characters. The code for each of the 2 characters will be the code for the *super character* followed by a 0 for one character and 1 for the other. Now delete the 2 least frequently used characters from the list and insert the new *super character* into the list at the appropriate place for its frequency. Continue this process until all characters and *super characters* are combined into 1 *super character*. The result is a Huffman code of minimal average code length. The Huffman code may best be seen as a binary tree with the terminal nodes (leaves) being the characters which are encoded.

Huffman coding can be quite successful in text compression, in extreme cases reducing the size of a file more than half. The basic technique can be improved upon in a number of ways. For example, pairs of characters, rather than single characters, can be used as the basis of encoding. This requires a much larger table of character frequencies, since now we need to compute the frequencies of character pairs, and larger tables of character pair and Huffman code associations, but can result in greater savings.

Another possibility is to use conditional Huffman coding. The objective here is to utilize the fact that the probability (frequency) of a character will vary depending upon what character precedes it. For example, compare the probability of a *U* following a *Q* (nearly 1) to the probability of a *U* following a *U* (nearly 0). So an optimal encoding should use a very short code for a *U* which follows *Q* and can use a very long code for a *U* which follows a *U*. The encoding algorithm involves computing the frequency with which each character follows every other character. A separate Huffman code is then computed for the characters which follow each character. The encoding scheme remembers the last character encoded and uses that to select the code to be used for the next character. The decoding algorithm must also remember the last character decoded in order to be able to select the correct decoding algorithm.

Huffman codes are really quite simple, but they can be made more sophisticated to achieve increased text compression. However, even with simple Huffman codes, some problems can arise. First, notice that Huffman encoding and decoding both involve a great deal of bit manipulation, which can be very slow to program. Second, the best compression is achieved if a Huffman code can take advantage of the unequal fre-

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Animation by Michael Smith
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quencies of characters in a file, but these will differ from file to file. Thus a separate encoding may be best for each file. This can be done by appending the code at the front of a file (as with the dictionaries used for abbreviations) but this increases the size of the file (significantly for small files).

Third, the variable length code nature of Huffman coding can make them extremely vulnerable to transmission or storage errors. In a fixed length code, if 1 bit is changed, only that 1 character is affected, while with Huffman codes, both that character and all succeeding characters may be decoded incorrectly because of a mistake in the assumed length of the incorrect character. (A similar problem would happen to a fixed length code if a bit were dropped or added.) Thus, for safety, it is necessary to add error detection and correction redundancy back into the file, increasing its size.

Still there are environments in which Huffman coding can be quite useful. Consider a word processing system storing files on a low speed serial device such as a cassette. Since the system is special purpose, one can compute the expected frequencies of English characters and use 1 Huffman code for all files. Encoding and decoding would be done automatically by the tape driver routines. Alternatively the encoding and decoding could be built into the tape drive hardware itself as special purpose logic or a small processor with a read only memory encoding/decoding table. This encoding/decoding approach would be totally transparent to the user. The only effect on the user would be the ability to store a larger, but variable number of "characters" on a fixed amount of tape.

Conclusions

The amount of storage space needed to store information can be greatly reduced by simple text compression techniques like the ones we have presented here. Each of the techniques presented can save some space in many files. And many of the techniques can be used one after another to achieve more and more compression. Text compression can be a simple and effective method of increasing the amount of storage available in exchange for some processor cycles. ■

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Selectable condensed character set	**Yes**	No	No	No	Yes	Yes
Full function VFU	**Yes**	Yes	No	No	Yes	No
Built-in self test	**Yes**	No	No	No	Yes	No
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Analysis of Polynomial Functions with the TI-59 Calculator

Part 1

Pierre Chancé
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Between the elementary functions accessible by direct calculation and higher-order equations reserved for the computer, there exists an intermediate domain where programmable calculators are useful.

Certain concrete problems sometimes lead to such equations without this creating an exceptional volume of calculation. Some have been encountered, for example, in the handling of small 6 by 6 matrices concerning medical data. Other technicians are also familiar with this type of obstacle in their fields. Consequently, the feeling is that it is worthwhile proposing a convenient program worked out on the Texas Instruments TI-59 and designed for sixth-order and lower-degree polynomial functions.

Independent of the advantages in mathematical terms, I hope that this article will give the user a meaningful introduction to this highly advanced calculator. For practical reasons, the original goals were as follows:

- calculate all the characteristic elements of the function (roots, maximums, minimums, and points of inflection where applicable)
- automatically plot the function curve
- control the program with a single key

Obtaining these conditions virtually eliminates any chance of operating error, and frees the user for other tasks once the calculation has begun. This is especially the case since the main program can be stored on a single magnetic card as can the printout program. Altogether, this provides a simplified procedure which nonetheless permits execution of the successive steps in the following sequence:

- obtaining the appropriate boundaries of the interval to be studied
- choice of the increment
- recall of the maximum error
- calculation of roots in increasing order
- printout of correctly sampled tables of values

All of the above is applicable both for the initial polynomial and for derived polynomials. Because of the geometric significance of the derivative, these provide the maximums and minimums of the function as well as possible points of inflection.

Given that excessive automation can be inconvenient in certain cases, a manual procedure has been provided to permit using the keys to enter the lower and upper boundaries of the interval to be studied along with the value of the increment desired.

After a brief discussion of the calculation principles, the main program and then the automatic printout program for the function curve will be examined. A commentary on numerical applications will conclude the examination.

Calculation Principles

Here is the type of polynomial that will be dealt with:

$$P(x) = a_0x^n + a_1x^{n-1} + \ldots + a_n \quad (a_0 \neq 0,\ n \leq 6)$$

where x is a real number and coefficients $a_0, a_1, \ldots a_n$, are known real numbers.

The method used to determine the roots of $P(x) = 0$ is



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bipartition. This consists of successive dichotomies of the interval (a, b) chosen with the function being continuous over this interval. The calculation is performed sequentially, and the step increment is designated by $\triangle x$.

To determine the root of the equation which belongs to the segment $\triangle x$, the latter is divided in two, and the calculator retains that half at whose extremes the function has opposite signs. The new shortened segment is further divided in two, and the process is repeated iteratively until the upper value of the residual interval is limited by the error limit. The middle of this final interval represents a root of the function to within the error.

This method provides only a single value in an interval $\triangle x$ and requires more calculating time if boundaries a and b are taken too far apart. If they are taken too close together, the risk is obviously one of losing a root; the same applies if $\triangle x$ is too large. Therefore we attempt to eliminate these drawbacks due to too much and too little by programming Lagrange's theorem. This replaces a subjective estimation of the boundaries by a calculation guaranteeing a reliable interval (a, b).

Let $a_0 > 0$ and a_k ($k \geq 1$) be the first of the negative coefficients of the polynomial P(x). The following number as the upper limit of the positive roots of equation $P(x) = 0$ can then be used:

$$R = 1 + \sqrt[k]{\frac{B}{a_0}}$$

where B is the largest of the absolute values of the negative coefficients of the polynomial P(x). Now the user no longer has to distinguish the two values of x between which the roots are supposed to fall. The calculator finds and prints them. To determine the possible limit of the negative roots of the equation, use $x = -z$. This involves changing the sign of the coefficients of the odd registers. However, if the latter equation has no positive roots, the initial equation has no negative roots and the calculator will not provide any.

Optimization of the process is completed by another method. As soon as a root is found, it serves as the lower boundary of the cycle of the following calculation. This sets the increment interval in the new segment to be explored. The correction is aimed at improving the reliability of root detection: this is an essential point.

Observe that details of the program code depend on some of the special capabilities of the TI-59 and PC-100A printing cradle. Naturally, the reader is referred to the instruction manual for full details. In passing, it is merely my intention to mention the decisive factors in my work.

The user has 960 program statements or 100 storage locations available with the possibility of adjusting their respective size as a function of the problem. Each memory block occupies eight program statements. The standard distribution adopted uses 480 program statements and sixty data-storage locations which will be filled entirely. The micromemory connects to the calculator and provides a library of twenty-five programs totalling 5000 steps.

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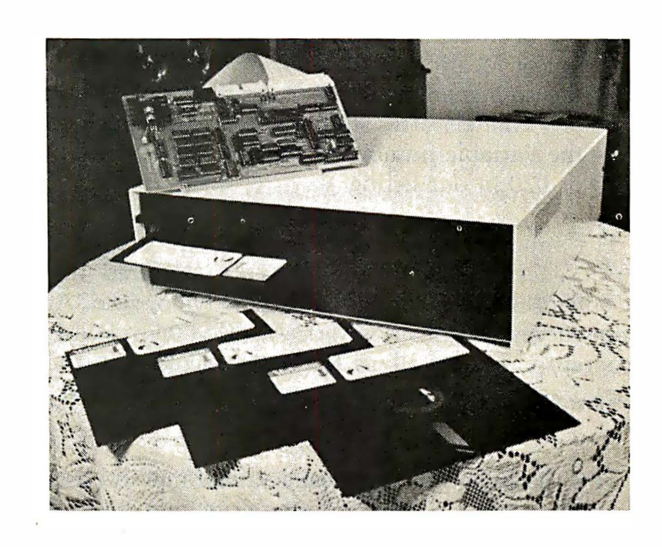
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access, special mention can be made of the following:

- printout of alphanumeric characters
- sign indicator
- error indicator
- incrementing and decrementing of memories
- listing of memory content
- listing of labels

Lastly, the T register is very important. Here, it is possible to store and recall a number and test it with respect to the contents of the display register.

In the final analysis, the TI-59 has the quantitative and qualitative features which prove useful in writing a program of the type that is being presented.

Main Program

Data entry:

For reasons of efficiency, the initialization sequence and data entry is not placed at the beginning of the program but at statement 066 with the LBL A instruction and statement 073 with the LBL B instruction (see listing 1). The coefficients of the polynomial are stored by conventional indirect addressing from x^6 at R_{16} to x^0 at R_{10} with a zero introduced when a corresponding term of a power of x is missing.

Evaluation of the polynomial:

This is the role of the LBL A′ instruction placed at location 000 to save calculating time, since this sequence is called frequently.

Determination of boundaries and step increment:

The calculation is monitored by LBL C which, in particular, uses subroutines RCL and STO and PGM 08 of the Solid-State Software. After execution of the sequences the following results are given:

- the lower boundary a is printed out at location 091
- the upper boundary b is printed out at location 099
- the absolute value of the interval (b-a) is printed out at location 117
- the step increment $\triangle x$ is printed out at step 124 immediately after steps 120 thru 122 which contain the variable number of partitions of interval (a, b) or 020 in our listing

The appearance of a zero as a boundary value means the absence of roots for the interval considered, the coefficients of the polynomial being positive or zero. And by three successive calls (PGM 08 A, PGM 08 B, PGM 08 C) program C finally aligns the assignments with those of the library by storing a at R_{01}, b at R_{02} and $\triangle x$ at R_{03}.

Program execution:

This discussion of the mathematical method used will save the trouble of describing the principles again. As for execution:

- LBL RCL (statement 133) changes the sign of the coefficients of the odd registers (R_{15}, R_{13}, R_{11})
- LBL STO (statement 155) plays a complex role. At statement 176, it stores the first coefficient which is

Listing 1: *Main program listing of the polynomial-function analysis on the TI-59.*

```
000 76 LBL     104 11  A      208 77  GE     312 99 PRT
001 16 A'      105 43 RCL     209 02  02     313 69 OP
002 53  (      106 18  18     210 20  20     314 18  18
003 42 STO     107 36 PGM     211 69 OP      315 87 IFF
004 17  17     108 08  08     212 31  31     316 07  07
005 69 OP      109 12  B      213 97 DSZ     317 02  02
006 10  10     110 98 ADV     214 00  00     318 96  96
007 42 STO     111 43 RCL     215 02  02     319 98 ADV
008 18  18     112 18  18     216 05  05     320 18 C'
009 43 RCL     113 75  -      217 00  0      321 92 RTN
010 01  01     114 43 RCL     218 92 RTN     322 76 LBL
011 42 STO     115 17  17     219 50 I×I     323 18 C'
012 19  19     116 95  =      220 42 STO     324 24 CE
013 06  6      117 99 PRT     221 07  07     325 43 RCL
014 42 STO     118 55  ÷      222 43 RCL     326 02  02
015 00  00     119 68 NOP     223 00  00     327 75  -
016 01  1      120 00  0      224 42 STO     328 93  .
017 06  6      121 02  2      225 02  02     329 05  5
018 42 STO     122 00  0      226 94 +/-     330 49 PRD
019 01  01     123 95  =      227 85  +      331 03  03
020 43 RCL     124 99 PRT     228 43 RCL     332 43 RCL
021 17  17     125 36 PGM     229 20  20     333 03  03
022 45 Y×      126 08  08     230 95  =      334 65  ×
023 43 RCL     127 13  C      231 42 STO     335 03  3
024 00  00     128 98 ADV     232 20  20     336 09  9
025 65  ×      129 19 D'      233 43 RCL     337 95  =
026 24 CE      130 15  E      234 02  02     338 42 STO
027 73 RC*     131 92 RTN     235 42 STO     339 01  01
028 01  01     132 76 LBL     236 00  00     340 02  2
029 69 OP      133 43 RCL     237 85  +      341 01  1
030 30  30     134 01  1      238 09  9      342 42 STO
031 69 OP      135 05  5      239 95  =      343 00  00
032 31  31     136 42 STO     240 42 STO     344 03  3
033 85  +      137 01  01     241 01  01     345 09  9
034 43 RCL     138 03  3      242 29 CP      346 42 STO
035 17  17     139 42 STO     243 73 RC*     347 09  09
036 45 Y×      140 00  00     244 01  01     348 43 RCL
037 43 RCL     141 01  1      245 22 INV     349 01  01
038 00  00     142 94 +/-     246 77  GE     350 72 ST*
039 65  ×      143 64 PD*     247 02  02     351 00  00
040 24 CE      144 01  01     248 67  67     352 69 OP
041 43 RCL     145 02  2      249 69 OP      353 20  20
042 18  8      146 22 INV     250 31  31     354 43 RCL
043 65         147 44 SUM     251 97 DSZ     355 03  03
044 73 RC*     148 01  01     252 00  00     356 44 SUM
045 01  01     149 97 DSZ     253 02  02     357 01  01
046 85  +      150 00  00     254 42  42     358 97 DSZ
047 69 OP      151 01  01     255 01  1      359 09  09
048 31  31     152 41  41     256 85  +      360 03  03
049 97 DSZ     153 92 RTN     257 43 RCL     361 48  48
050 00  00     154 76 LBL     258 07  07     362 24 CE
051 00  00     155 42 STO     259 22 INV     363 02  2
052 20  20     156 07  7      260 45 Y×      364 01  1
053 43 RCL     157 42 STO     261 43 RCL     365 22 INV
054 10  10     158 00  00     262 20  20     366 90 LST
055 54  )      159 01  1      263 95  =      367 24 CE
056 42 STO     160 06  6      264 42 STO     368 98 ADV
057 17  17     161 42 STO     265 02  02     369 02  2
058 43 RCL     162 01  01     266 92 RTN     370 01  1
059 19  19     163 29 CP      267 50 I×I     371 42 STO
060 42 STO     164 73 RC*     268 32 X:T     372 09  09
061 01  01     165 01  01     269 43 RCL     373 22 INV
062 43 RCL     166 22 INV     270 07  07     374 86 STF
063 17  17     167 67  EQ     271 77  GE     375 07  07
064 92 RTN     168 01  01     272 02  02     376 73 RC*
065 76 LBL     169 76  76     273 49  49     377 09  09
066 11  A      170 69 OP      274 73 RC*     378 16 A'
067 01  1      171 31  31     275 01  01     379 72 ST*
068 06  6      172 97 DSZ     276 50 I×I     380 09  09
069 42 STO     173 00  00     277 42 STO     381 69 OP
070 00  00     174 01  01     278 07  07     382 29  29
071 92 RTN     175 64  64     279 61 GTO     383 69 OP
072 76 LBL     176 42 STO     280 02  02     384 18  18
073 12  B      177 07  07     281 49  49     385 87 IFF
074 72 ST*     178 43 RCL     282 76 LBL     386 07  07
075 00  00     179 00  00     283 14  D      387 03  03
076 99 PRT     180 42 STO     284 99 PRT     388 73  73
077 69 OP      181 20  20     285 36 PGM     389 24 CE
078 30  30     182 73 RC*     286 08  08     390 02  2
079 92 RTN     183 01  01     287 14  D      391 01  1
080 76 LBL     184 55  ÷      288 98 ADV     392 22 INV
081 13  C      185 43 RCL     289 92 RTN     393 90 LST
082 98 ADV     186 07  07     290 76 LBL     394 98 ADV
083 71 SBR     187 95  =      291 15  E      395 98 ADV
084 43 RCL     188 72 ST*     292 36 PGM     396 98 ADV
085 71 SBR     189 01  01     293 08  08     397 92 RTN
086 42 STO     190 69 OP      294 15  E      398 76 LBL
087 68 NOP     191 31  31     295 99 PRT     399 19 D'
088 94 +/-     192 97 DSZ     296 22 INV     400 93  .
089 42 STO     193 00  00     297 86 STF     401 00  0
090 17  17     194 01  01     298 07  07     402 00  0
091 99 PRT     195 82  82     299 85  +      403 00  0
092 71 SBR     196 43 RCL     300 43 RCL     404 00  0
093 43 RCL     197 20  20     301 08  08     405 00  0
094 71 SBR     198 42 STO     302 65  ×      406 01  1
095 42 STO     199 00  00     303 01  1      407 68 NOP
096 68 NOP     200 85  +      304 00  0      408 68 NOP
097 42 STO     201 09  9      305 95  =      409 68 NOP
098 18  18     202 95  =      306 36 PGM     410 68 NOP
099 99 PRT     203 42 STO     307 08  08     411 14  D
100 43 RCL     204 01  01     308 11  A      412 92 RTN
101 17  17     205 73 RC*     309 36 PGM     413 76 LBL
102 36 PGM     206 01  01     310 08  08     414 17 B'
103 08  08     207 22 INV     311 15  E      415 43 RCL
```

Listing 1 continued on page 126

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Listing 1 continued:

```
416  11  11     436  04   4     456  16  16     476  10  10
417  42 STO     437  95   =     457  43 RCL     477  99 PRT
418  10  10     438  42 STO     458  16  16     478  98 ADV
419  43 RCL     439  13  13     459  99 PRT     479  92 RTN
420  12  12     440  43 RCL     460  43 RCL
421  65   ×     441  15  15     461  15  15
422  02   2     442  65   ×     462  99 PRT
423  95   =     443  05   5     463  43 RCL
424  42 STO     444  95   =     464  14  14     001  16  A'
425  11  11     445  42 STO     465  99 PRT     066  11   A
426  43 RCL     446  14  14     466  43 RCL     073  12   B
427  13  13     447  43 RCL     467  13  13     081  13   C
428  65   ×     448  16  16     468  99 PRT     133  43 RCL
429  03   3     449  65   ×     469  43 RCL     155  42 STO
430  95   =     450  06   6     470  12  12     283  14   D
431  42 STO     451  95   =     471  99 PRT     291  15   E
432  12  12     452  42 STO     472  43 RCL     323  18  C'
433  43 RCL     453  15  15     473  11  11     399  19  D'
434  14  14     454  00   0     474  99 PRT     414  17  B'
435  65   ×     455  42 STO     475  43 RCL
```

not zero in register R_{07} and recalls its rank in R_{00} to store it at STO 20.

At statements 182 thru 192, all the terms of the polynomial, starting with the first, are divided by the first coefficient which is not zero. This make a_0 positive and equal to 1. This operation must be kept in mind to correctly interpret the change from one polynomial to the next when reading the results.

Location of the first negative coefficient to determine its value and rank begins at statement 196 and uses two loops, statements 203 thru 205 and 207 thru 219. Finally, if the negative coefficient exists, its absolute value is stored in register R_{07} and its rank in register R_{02}, and then its relative position with respect to the first coefficient which is not zero is stored in register R_{20}. Incidentally, the register number of a coefficient (R_{01}) can be determined easily by adding 9 to its ordinal number (R_{00}).

The calculation of the negative coefficient which has the highest absolute value starts at statement 233 and uses the T register with a relatively sophisticated process. This employs four loops, 251 thru 242, 245 thru 267, 271 thru 249 and 279 thru 249. The evaluation of R in Lagrange's formula takes place at statements 255 thru 265.

On the whole, the STO program can be considered to end with the RTN instruction of statement 218 with a long conditional branch with multiple options which operates as a subroutine and ends at the RTN of statement 266.

Maximum error:

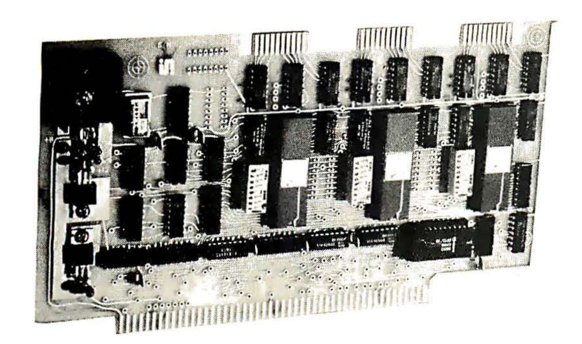
This factor is introduced by LBL D (statement 283) which is none other than the assignment of the error ϵ in R_{03} in accordance with the assignment of PGM 08 D in the library. From experience it can be seen that repetition of the error coefficient for each calculation sequence constitutes a constraint, and that setting it at 0.01 in the absence of error entry, as provided by PGM 08, does not really spare the user from this preoccupation.

The fact is that although the precision required varies from one operator to the next, everyone generally uses a rather constant factor for a series of calculations.

It is thus practical to keep ϵ in the program, even if this means modifying it to the programming mode as soon as the need arises. This is the role of LBL D′ (statement 399) where statements 400 thru 410 can contain ϵ up to 1×10^{-10} unless less precision is preferred. It is then sufficient to fill the empty spaces with NOP instructions or simply with zeros after the first significant figure. Since LBL D′ calls D at statement 411 but is itself called by C at

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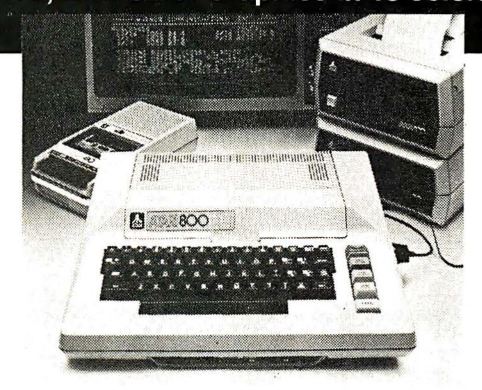
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statement 129, it is clear that key C finally controls recall, printout and then entry of the maximum error ϵ programmed by the operator.

Calculation of roots:

The heart of this calculation is PGM 08 E from the library which we call at statements 292 and 309. Determination of the successive roots is implemented by our LBL E (statement 291). From the second root, the lower boundary a takes the value of the preceding root augmented by a minimum quantity equal to $\epsilon \times 10$. This augmentation is an artifice designed to move the calculator off the solution it has just found.

The process continues up to unsuccessful exploration of the last interval. At printout this initiates the characteristic series of 9.999...? provided by the manufacturer's PGM 08. LBL E itself is controlled by LBL C at statement 130. This is why key C in fact initiates determination of the roots at the right time.

Tables of values of x and P(x):

These two tables are successively printed out by LBL C′ (statement 323) which samples thirty-nine suitable stored values of x from registers R_{21} thru R_{59} and replaces them immediately in the same registers with the thirty-nine corresponding values of P(x). The median of x may be very close to zero. This means that the median of P(x) corresponds to the value of the polynomial for $x = 0$ when $P(x) = P(-x)$.

The sequence C′ starts with restoration of the lower boundary a in R_{01} and stores a new increment in R_{03} taken from forty statements between a and b. An automatic listing of the memories with loop and error-indicator control provides indexing of the values.

Sequence C′ is itself controlled by LBL E at statement 320 after FLAG 07 has used the error signal from the end of root determination. Given that LBL E is subordinate to LBL C, as was stated earlier, sequence C′ is finally implemented by key C also. Given the partition used, the thirty-nine sample values of x and then of P(x) occupy statements 480 thru 959. Those of P(x) can be recorded on a magnetic card in groups 3 and 4 for automatic printout by points of the function curve. The polynomials derived from P(x) could obviously be recorded in the same manner.

Calculation of derived polynomials:

The derivation of each polynomial term of the general expression ax^n gives a term of the expression anx^{n-1}. The calculation is performed by LBL B′ (statement 414) which, by depressing key B′ once, prints out all the coefficients from x^6 to x^0. The sequence has been designed to provide P′(x) from P(x), P″(x) from P′(x) and so forth as long as the polynomial remains differentiable. Since the program then divides the polynomial by its first nonzero coefficient, it will come as no surprise to find a derivative divided by this term. This in no way changes the final results.

As soon as key B′ has played its role, it is sufficient to depress key C for the derived polynomial to be handled in accordance with the same complete cycle as described for the initial polynomial. No other intervention is necessary, unless it is desired to return to the initial

polynomial to evaluate it as a function of the roots found for the derived polynomials. This determination is only made after all the derived polynomials that are deemed useful have been used in sequence by the automatic procedure just indicated.

When the coefficients of the initial polynomial have been reentered from R_{16} to R_{10} as at the beginning, enter each root on the keyboard, and each time depress A′. This evaluates the corresponding P(x). The function curve is then completed by virtue of the geometric significance of the derivative by the following coordinates:

- to the root of P′(x) = 0 taken as the abscissa corresponds an ordinate by P(x) which defines a maximum or minimum of P(x) = 0
- to the root of P″(x) = 0 taken as the abscissa corresponds an ordinate by P(x) which defines a point of inflection of P(x) = 0 if there is one

Program of Function Curve

Principle:

The curve of the polynomial is automatically plotted as shown in the program in listing 2. It was necessary to conceive an algorithm that compensates for the relative weakness of the TI-59 in this area, since it accepts only twenty whole positive values on a 2.5 inch tape.

With the exception of special cases, the spacing of the plotted points is manifestly insufficient. It can be seen that to cover an 8.5 by 14 inch sheet of paper (a standard European A4 sheet, 21 by 29.7 cm), six strips of machine

Listing 2: *Listing of the program that will plot the function curve.*

```
000  76 LBL
001  98 ADV
002  69 OP
003  00  00
004  04  4
005  00  0
006  00  0
007  00  0
008  00  0
009  00  0
010  00  0
011  00  0
012  00  0
013  00  0
014  69 OP
015  01  01
016  69 OP
017  05  05
018  92 RTN
019  76 LBL
020  28 LOG
021  73 RC*
022  00  00
023  75  -
024  43 RCL
025  20  20
026  95  =
027  69 OP
028  07  07
029  43 RCL
030  06  06
031  65  ×
032  07  7
033  95  =
034  72 ST*
035  00  00
036  92 RTN
037  76 LBL
038  75  -
039  22 INV
040  77  GE
041  00  00
042  21  21
043  71 SBR
044  95  =
045  92 RTN
046  76 LBL
047  11  A
048  07  7
049  42 STO
050  00  00
051  92 RTN
052  76 LBL
053  12  B
054  50 I×I
055  72 ST*
056  00  00
057  55  ÷
058  01  1
059  00  0
060  95  =
061  74 SM*
062  00  00
063  69 OP
064  20  20
065  92 RTN
066  76 LBL
067  13  C
068  14  D
069  15  E
070  92 RTN
071  76 LBL
072  14  D
073  03  3
074  09  9
075  42 STO
076  09  09
077  02  2
078  01  1
079  42 STO
080  00  00
081  53  (
082  73 RC*
083  00  00
084  55  ÷
085  43 RCL
086  03  03
087  85  +
088  43 RCL
089  07  07
090  55  ÷
091  43 RCL
092  03  03
093  54  )
094  65  ×
095  53  (
096  53  (
097  43 RCL
098  03  03
099  65  ×
100  01  1
101  09  9
102  93  .
103  08  8
104  65  ×
105  06  6
106  54  )
107  55  ÷
108  53  (
109  43 RCL
110  07  07
111  85  +
112  43 RCL
113  08  08
114  54  )
115  54  )
116  95  =
117  72 ST*
118  00  00
119  69 OP
120  20  20
121  97 DSZ
122  09  09
123  00  00
124  81  81
125  92 RTN
126  76 LBL
127  15  E
128  53  (
129  43 RCL
130  07  07
131  85  +
132  43 RCL
133  08  08
134  54  )
135  55  ÷
136  06  6
137  55  ÷
138  43 RCL
139  03  03
140  95  =
141  42 STO
142  06  06
143  06  6
144  42 STO
145  05  05
146  00  0
147  42 STO
148  01  01
149  29 CP
150  02  2
151  01  1
152  42 STO
153  00  00
154  03  3
155  09  9
156  42 STO
157  09  09
158  43 RCL
159  06  06
160  65  ×
161  43 RCL
162  01  01
163  95  =
164  42 STO
165  20  20
166  69 OP
167  21  21
168  43 RCL
169  06  06
170  65  ×
171  43 RCL
172  01  01
173  99 PRT
174  98 ADV
175  98 ADV
176  98 ADV
177  95  =
178  32 X↕T
179  73 RC*
180  00  00
181  71 SBR
182  75  -
183  69 OP
184  20  20
185  97 DSZ
186  09  09
187  01  01
188  79  79
189  98 ADV
190  98 ADV
191  10 E'
192  98 ADV
193  98 ADV
194  98 ADV
195  97 DSZ
196  05  05
197  01  01
198  49  49
199  92 RTN
200  76 LBL
201  99 PRT
202  69 OP
203  00  00
204  07  7
205  05  5
206  00  0
207  00  0
208  00  0
209  00  0
210  00  0
211  00  0
212  00  0
213  00  0
214  69 OP
215  01  01
216  69 OP
217  05  05
218  92 RTN
219  76 LBL
220  95  =
221  00  0
222  32 X↕T
223  43 RCL
224  00  00
225  75  -
226  04  4
227  00  0
228  95  =
229  67  EQ
230  02  02
231  02  02
232  71 SBR
233  36 PGM
234  43 RCL
235  06  06
236  65  ×
237  43 RCL
238  01  01
239  95  =
240  32 X↕T
241  92 RTN
242  76 LBL
243  36 PGM
244  22 INV
245  67  EQ
246  00  00
247  02  02
248  92 RTN
249  76 LBL
250  10 E'
251  69 OP
252  00  00
253  19 D'
254  69 OP
255  01  01
256  19 D'
257  69 OP
258  02  02
259  19 D'
260  69 OP
261  03  03
262  19 D'
263  69 OP
264  04  04
265  69 OP
266  05  05
267  92 RTN
268  76 LBL
269  19 D'
270  04  4
271  00  0
272  04  4
273  00  0
274  04  4
275  00  0
276  04  4
277  00  0
278  04  4
279  00  0
280  92 RTN

001  98 ADV
020  28 LOG
038  75  -
047  11  A
053  12  B
067  13  C
072  14  D
127  15  E
201  99 PRT
220  95  =
243  36 PGM
250  10 E'
269  19 D'
```



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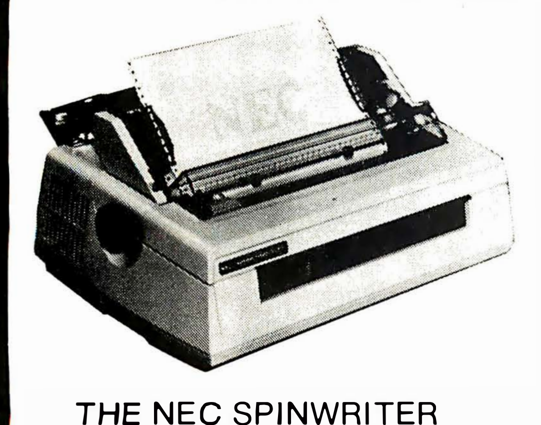
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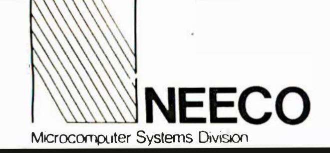
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paper must be juxtaposed. In practice, this means making the data positive, preparing a suitable format and then dividing it into six parts. Thus, the calculator can sequentially print the asterisks corresponding to the thirty-nine values of registers R_{21} thru R_{59}. This can be accomplished in six runs.

Since asterisks will be printed for only thirty-nine pieces of data on 39 by 6 runs, a printout arrangement by points on the base line is used to mark the nonoperation. The interval between points is equal to the increment of the table of the values of x.

Location in the plane is completed by two other arrangements:

- a sign in the shape of a triangle, in place of a point, marks the middle of the base line when there is no value on the zero abscissa
- the ordinates are marked laterally by a column of points with twenty per tape

Initialization and data entry:

These operations are performed by LBL A (statement 047) and LBL B (statement 053). The lower data item entered first is stored in register R_{07}, and the upper data item, entered second, is stored in register R_{08}. The choice of these values determines the amplitude of the graphic reproduction. If it is desired to cover a maximum field, it is necessary to determine the extremes of the values to be reproduced by concurrently consulting the table of the values of P(x) and the group of values of P(x) for x taken from the roots of $P'(x) = 0$.

Note that LBL B continues (statement 057) with the addition of the tenth of each value entered. This automatically provides a margin for the sheet.

Service labels:

Since there is no point in spreading signs on a page without identification, a certain number of sequences permit projections along the abscissa and ordinates. LBL ADV (statement 001) prints one point on the base line of the strip when no data appears on the corresponding abscissa. You will recognize the alphanumeric code controlled by instructions OP 00, OP 01 and OP 05.

Instead of a point, LBL PRT (statement 201) prints a small triangle in the middle of the base line. This distinctive sign marks the zero abscissa when no data item corresponds to it. This median is recognized by monitoring register R_{40} in passing and, by subtracting its ordinal number, it checks for the zero condition using the T register ($=$ t or $\neq$ t). The conditional transfer is executed by means of the LBL = instruction at statement 220 and LBL PGM at statement 243 (the first being called as a subroutine at statement 043 by the LBL − instruction and the second at statement 232 by the LBL =instruction). Naturally, the T register is restored to its previous value immediately after statement 234 and before returning to the main program to serve in the test of the upper limit for the following data item.

Incidentally, it can be observed here that the user is dealing with a structure with four levels of subroutines (main program → SBR − → SBR = → SBR PGM → SBR PRT). The calculator can handle them with no difficulty, since it can accept up to six successive calls. The ordinate location is provided by LBL E' (statement 250), called at

statement 181, which prints a column of points at the end of the tape. For reasons of economy, the alphanumeric characters are grouped in LBL D' at statement 269 and recalled as a subroutine whenever needed.

Data printout:

LBL LOG (statement 020) prints an asterisk when the value of R^*_{00} recalled by indirect addressing is between the lower and upper limits of the tape considered. Printout uses a special instruction OP 07. Conditional transfer is provided by LBL — which transfers execution to LBL LOG if the data item is acceptable after subtracting the value of the lower limit stored in register R_{20}. Finally, the data item processed is excluded from the printing field by addition of the group of seven instructions of the tape format contained in register R_{06} (statements 029 thru 035).

Data conversion:

This operation is executed by LBL D (statement 072). It assigns the thirty-nine data items collected by recording in groups 3 and 4 of registers R_{21} thru R_{59} on completion of calculation of the initial P(x) polynomial. However, this could just as well be a polynomial derived for another calculation purpose. The positive value and formatting of this data for printout are obtained with a better spread by dividing them by the increment of the table of values of x contained in register R_{03}. Each converted data item replaces the previous data item term for term in the same register R_{21} thru R_{59}.

Tape printout:

Printout of the six tapes is controlled by LBL E (statement 127). This sequence begins with calculation of the tape format stored in register R_{06}. Tape indexing depends on register R_{01}, initially loaded with zero at statement 146, then incremented at statement 166 and printed at statement 173. The lower tape limit is calculated at statement 165 (STO 20) and the upper limit at statement 177 for loading in the T register.

Transfer to the test of the upper tape limit is executed by instruction SBR — at statement 181. The mechanism of LBL E uses a double loop:

- 149 thru 198 for register R_{09} for data counting loaded at 39
- 179 thru 185 for register R_{05} for tape counting loaded at 6

The entire system is actuated by simply depressing key C, since LBL C at statement 067 monitors D and E. Part 2 of this article will discuss the numerical applications of this program. Samples will be provided to illustrate the initialization and plotting procedures to be followed to output the function curve. ■

Glossary

Lagrange's method: Several theorems exist that can solve for the real root(s) of a polynomial equation by means of successive approximations. Lagrange's method obtains the real root using only integer calculations, thereby eliminating any roundoff error. This process is therefore very useful for separation of roots located in a small interval.

Minimizing Curve-Plotting Calculation

Timothy G Bowker
Systems Research Labratories Inc
2800 Indian Ripple Rd
Dayton OH 45440

Are you plotting the results of time-consuming calculations? The efficient routine described here will give you accurate curves with fewer calculated points.

This article is written for the most common type of plotter/software combinations which draw straight lines between calculated points. Figure 1 shows superimposed curves, both of which are plots of the function 2^X as an example. The smooth curve is produced using a very small $\triangle X$, while the other is created with a $\triangle X$ equal to 2. The marks below the X axis indicate the values of X (and $\triangle X$, between two marks) used for the non-smooth curve. A comparison of the two curves illustrates where the greatest error occurs. When $\triangle X$ is constant and large, and straight lines are drawn between calculated points, the accuracy of a plot is less in regions of sharper curvature. The accuracy decreases in regions of greater slope (given equal curvature and constant $\triangle X$) because the plotted line-segment length is greater at steeper slopes.

It is often desirable to have consistent accuracy throughout a plot, and yet minimize the number of points required to plot a curve (to minimize calculation and running time). In such a case, it would be more efficient to use small values of $\triangle X$ in regions of steep slope and/or sharp curvature, and large values of $\triangle X$ in regions of little slope and little curvature.

Ideally, $\triangle X$ could be adjusted so that with a minimum number of calculated points, a curve would be plotted (with discrete, straight-line segments) such that the curve appeared accurate. This result may be achieved as illustrated in figure 2. (Again, the $\triangle X$ values used are marked below the X axis.) Note the smaller number of points calculated in the low slope/low curvature ($X<0$) area of the curve. Compare this with figure 3 which was plotted with a constant $\triangle X$ of 0.1. Figure 2 has slightly better resolution at the steepest part of the curve ($\triangle X$ min $\cong 0.09$) as well as having been plotted with less than half the points required for figure 3.

Figure 4 sheds additional light on the technique. The plot is identical to figure 2 except that crosses have been marked at each plotted point. Note that line-segment lengths are similar at both ends of the plot (where curvature is slight) but that the value of $\triangle X$ on both ends is vastly different, as may be observed by the X_i markers below the X axis. Also note that where curvature is greater, $\triangle X$ is adjusted to yield shorter line-segment lengths (as around X = 2).

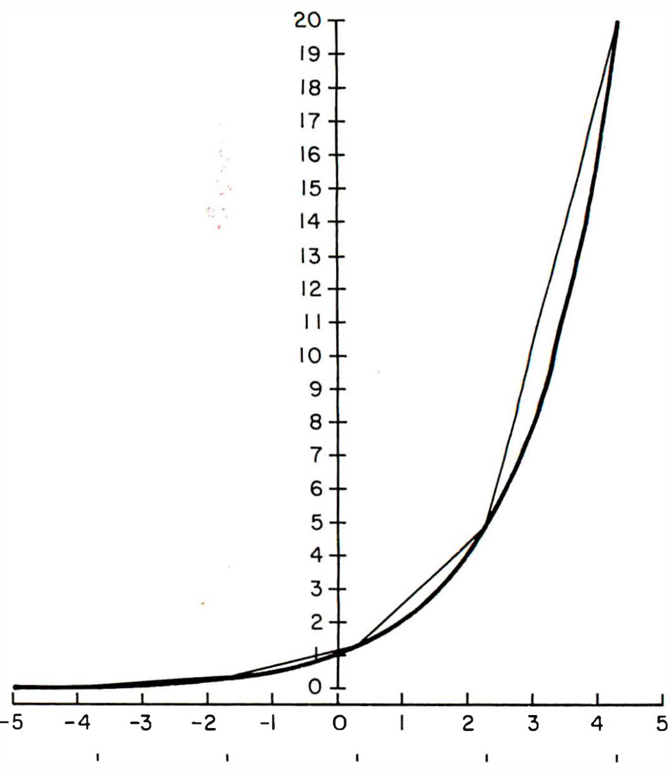


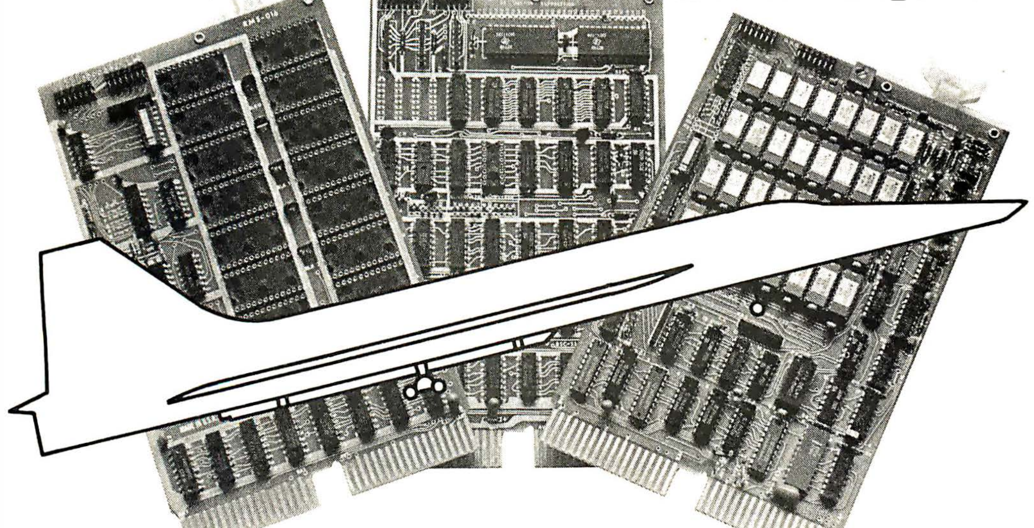
Figure 1: *True curve superimposed on curve plotted with $\triangle X=2$. Notice less accuracy in regions of greater slope or curvature using constant $\triangle X$.*

Figure 5 is a duplicate of figure 3, with crosses added at plotted points, which further emphasizes the effort wasted in low slope/low curvature areas using a constant $\triangle X$.

The Method

$\triangle X$ may be automatically varied during the running of a plotting program by estimating the curvature and slope

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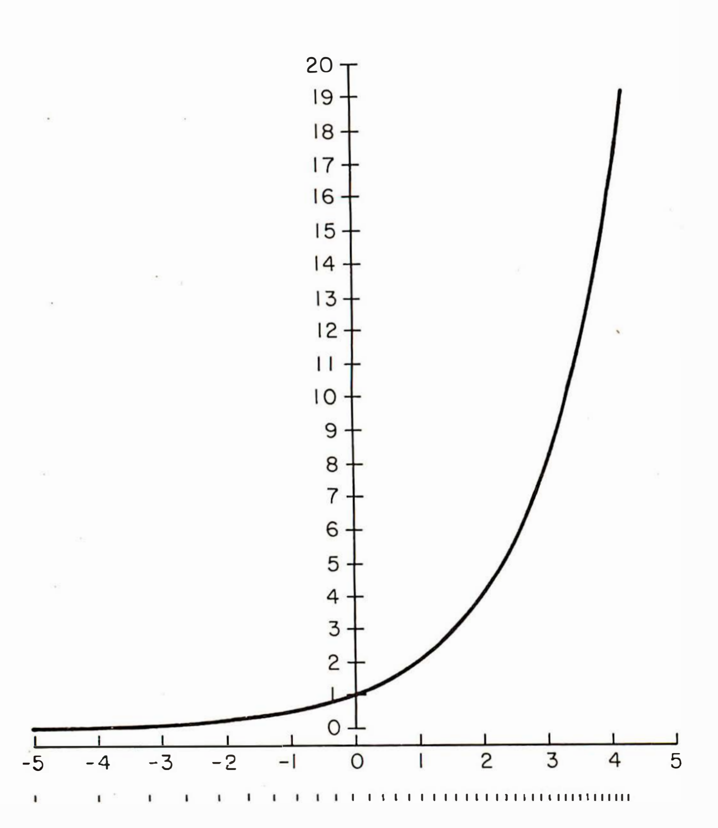


Figure 2: *Accurate curve plotted with more efficiently selected $\triangle X$ values (the increments for $\triangle X$ are indicated by marks below the X axis).*

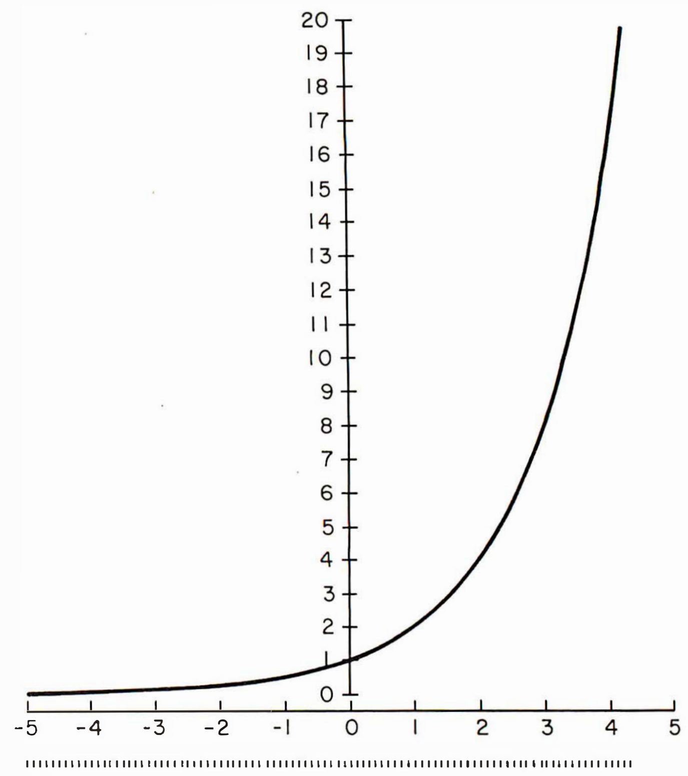


Figure 3: *Accurate curve plotted with constant $\triangle X$. Note the unnecessary points calculated and plotted in lower-left straight line portion of curve.*

of the upcoming curve. This is based on the slope of the last two plotted points and the curvature of the last three plotted points.

When there is no curvature, the plot segment length must still be limited, due to the look-back nature of the $\triangle X$ determination routine. In other words, the routine cannot assume that the rest of the plot is straight simply because the last portion was perfectly straight. Therefore, when dealing with a curve with no curvature, no matter what the slope, this routine will plot a line segment of approximately constant length. This length is selected by the programmer to accommodate the nature of the curve being plotted and resolution requirements.

This routine may be conveniently implemented using slope, trigonometric functions, angles, and changes in angle. A strictly geometric approach, while possibly appearing better than a trigonometric one, has serious difficulties.

The present routine stores the last two values of both X and Y and finds the appropriate "plot" slope of the last plotted curve segment. (It is necessary to be concerned with the slope as it appears plotted. The mathematical slope $(Y_i - Y_{i-1})/(X_i - X_{i-1})$ will probably not equal the plot slope due to difference between the X and Y scales. If 1 inch on the Y axis covers a $\triangle Y$ of M and 1 inch on the X axis covers a $\triangle X$ of N, then the mathematical slope, $\triangle Y/\triangle X$, should be multiplied by N/M to yield the plot slope. M and N should be fairly accurate for proper program operation.)

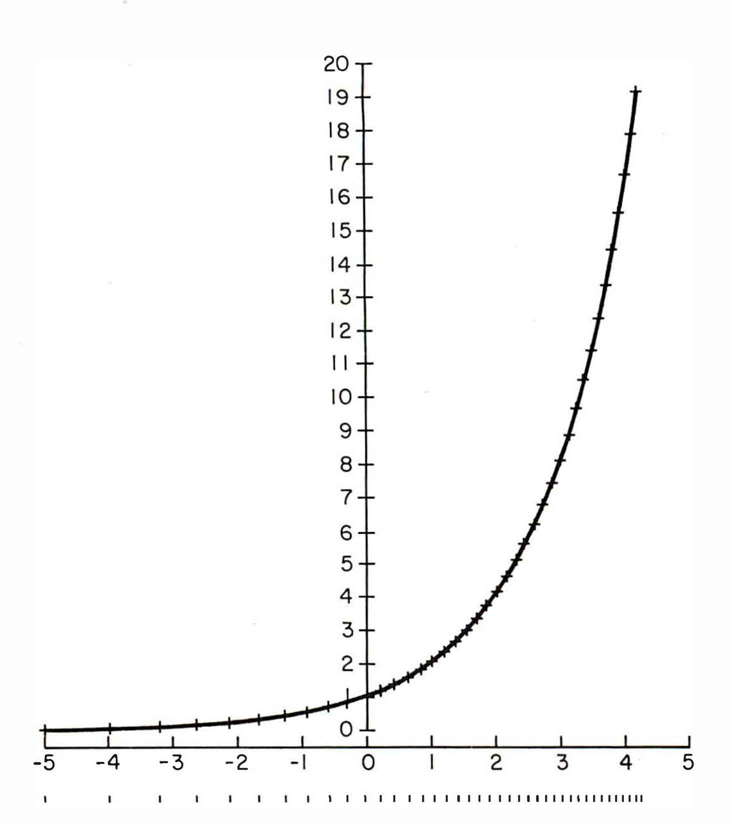


Figure 4: *Identical to figure 2 except that crosses are used to indicate plotted points. Note similar line segment lengths at both ends of the curve, but vastly different △X s (distances between marks below X axis). Note also the shorter line segments in area of greater curvature.*

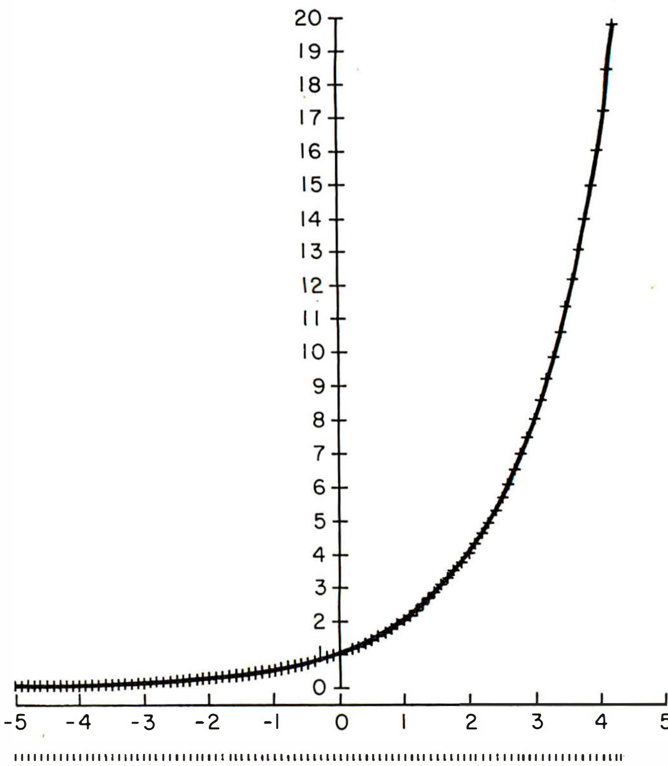


Figure 5: *Same as figure 3 with the crosses at all plotted points. Note the reasonable line segment lengths in the upper-right portion of curve, but unnecessarily short line segments in the lower left portion of curve due to the use of constant △X.*

The arctangent of the last plot slope is computed to yield the last plot angle. Taking the cosine of the last plot angle and multiplying by the value of the desired line-segment length (using X axis units) yields the required △X estimate for the next point as illustrated in figure 6. That is, when the last two line segments' curvature is zero:

$$\triangle X_i = X_{i+1} - X_i = L \cos \left\{ \arctan \left[\frac{N(Y_i - Y_{i-1})}{M(X_i - X_{i-1})} \right] \right\} \tag{1}$$

where:

L = desired maximum line-segment length,
N/M = scale difference adjustment factor.

This determines the contribution to △X from the plot slope (or first derivative) effects.

Notes on Figure 6

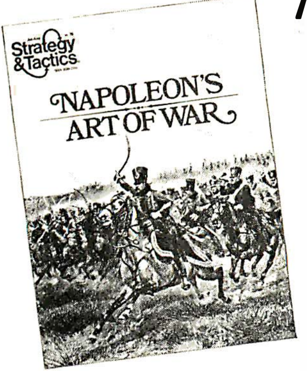
Assume (X_4, Y_4) and (X_5, Y_5) have been plotted, and $\triangle X_4$ and Q_4 (the corresponding slope angle) have been calculated, but that $\triangle X_5$, X_6, Y_6, and Q_5 are not yet known. It is assumed that Q_5 will be approximately equal to Q_4, which is generally true for small line-segment

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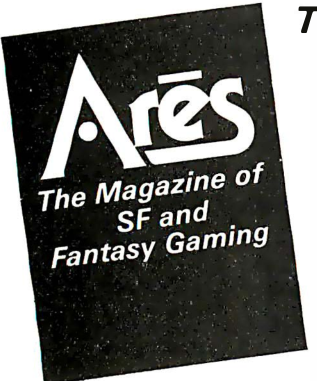
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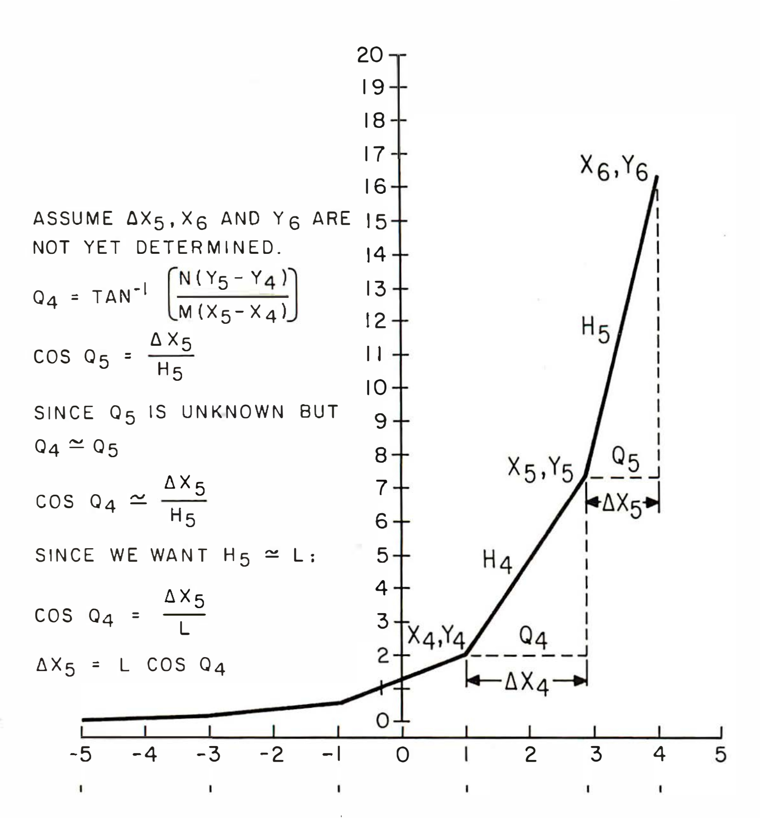


Figure 6: *Illustration of the trigonometric estimation of next ΔX, with no consideration of curvature. The line segment lengths have been exaggerated for demonstration purposes. The plot was run with the listed program with $L=2$ and $C=0$.*

lengths. Without considering curvature, you want H_5 to equal L, the desired line-segment length. From figure 6:

$$\frac{\Delta X_5}{H_5} = \cos Q_5$$

Assume $Q_4 \cong Q_5'$ so:

$$\frac{\Delta X_5}{H_5} \cong \cos Q_4$$

Substituting L for the desired value for H_5:

$$\frac{\Delta X_5}{L} = \cos Q_4$$

$$\Delta X_5 = L \cos Q_4$$

which is the estimate used for ΔX_5 to yield a line-segment length approximately equal to L, without consideration of curvature.

To adjust ΔX for curvature (or second derivative) effects, the plot angle of the last plotted curve segment is subtracted from the plot angle of the previously plotted curve segment to yield the change in plot angle. This value yields a direct indication of curvature, which is not, however, equal to the second derivative.

Since you are not concerned with the sign of the curvature, only its magnitude, take the absolute value of the change in plot angle. (You were not concerned with the sign of the slope either, but since this program is designed only for plots of single valued functions of "X" ($\Delta X > 0$), the cosine of the plot angle will always be positive, regardless of the sign of the slope, thus eliminating the need to take the absolute value.)

Taking equation 1 for ΔX without curvature and setting the plot angle equal to Q, you have:

$$\Delta X = L \cos Q \qquad (2)$$

for ΔX without curvature.

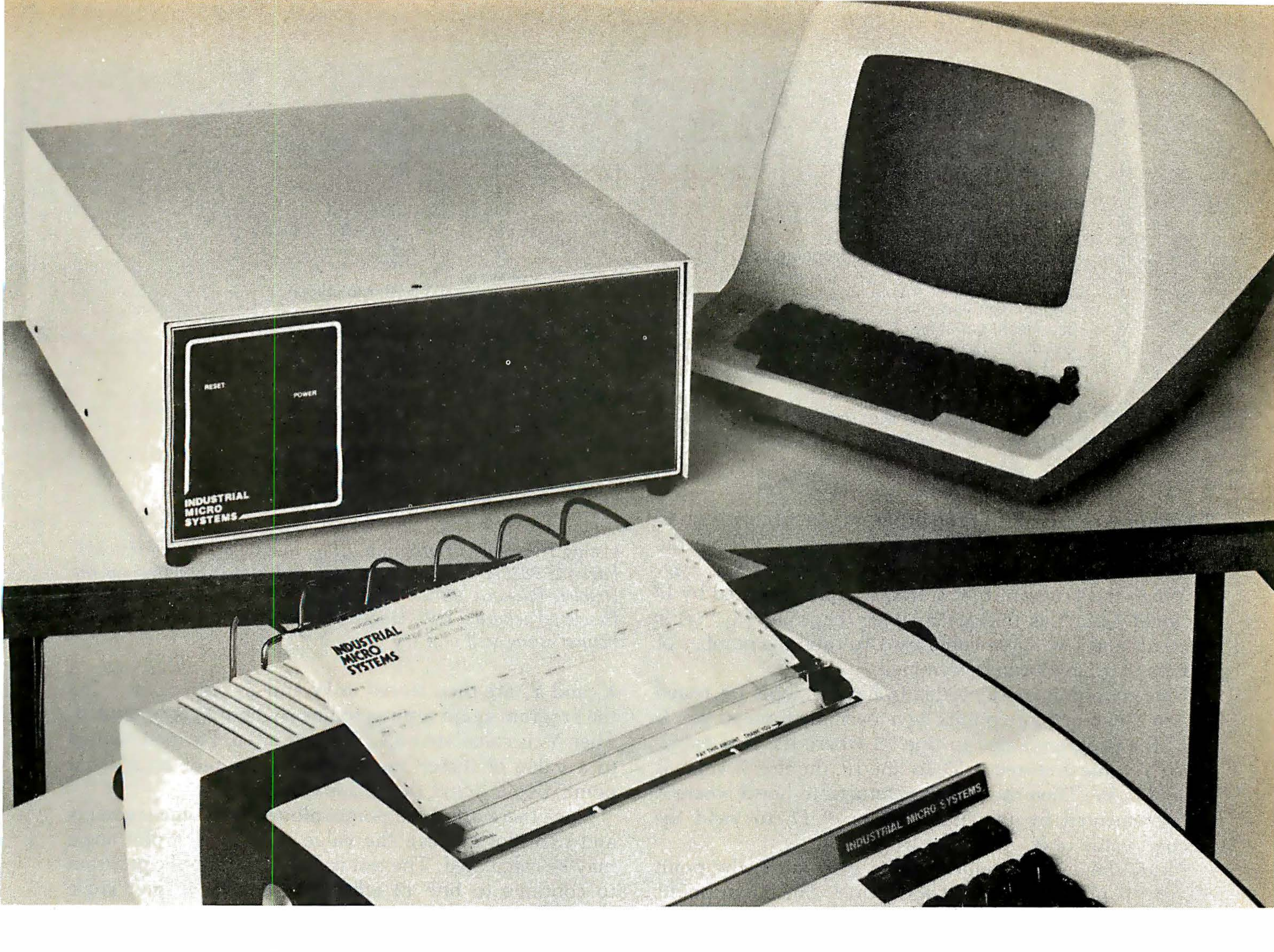
Perhaps the simplest way to include a contribution from the change in plot angle is in the following form:

$$\Delta X = \frac{L \cos Q}{1 + C(P-Q)} \qquad (3)$$

where C is a weighting factor which controls the effect of the change in plot angle (curvature) on ΔX, and P is the plot angle previous to the last plot angle, Q. Thus, $P-Q$ = the change in plot angle. It may be seen that equation 3 reduces to equation 2 when there is no curvature ($P = Q$, $P-Q = 0$). The weighting factor C is perhaps best determined by experimentation, but will probably be approximately equal to L when P and Q are in degrees.

Program Initialization and Operation

Since the program in listing 1 utilizes a look-back algorithm, some initialization is required because there are no "previous three points" at the beginning of the program.



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Variable List

C:	curvature weighting factor
D:	△X (variable X increment)
I:	points counter
L:	maximum line segment length
M:	units per inch on the Y axis
N:	units per inch on the X axis
P:	slope angle previous to last slope angle
Q:	last slope angle
W:	last independent variable
X:	independent variable
Y:	dependent variable
Z:	last dependent variable

Table 1: *List of variable definitions that are used in the plotting routine that outputs the curve in figure 2.*

```
0:   ent L,C
1:   4→M;2→N
2:   -5.01→X
3:   .01→D
4:   0→I
5:   "X=":X+D→X
6:   "Y=":2↑X→Y
7:   plt X,Y
8:   I+1→I
9:   if Y>20; gto "Stop"
10:  if I < 1.5; gto "Y→Z"
11:  atn ((N/M) (Y-Z)/(X-W))→Q
12:  if I<2.5; gto "Q→P"
13:  Lcos (Q)/(1+Cabs (P−Q))→D
14:  "Q→P":Q→P
15:  "Y→Z":Y→Z
16:  X→W
17:  gto "X="
18:  "Stop":stp
*32105
```

Listing 1: *Essence of program listing that will run on a Hewlett-Packard 9825A desktop computer and plot a function on the Hewlett-Packard 9872A plotter. The program is written in Hewlett-Packard's HPL language. The parameters in this particular listing will plot the curve in figure 2.*

Therefore, at the start of the program, an arbitrary small value (0.01 in the example) is assigned to △X (D in the program). I is initialized to zero and X is set to $X_{min} - D$.

When the program first starts, X is incremented by D to yield X_{min}. Y is then calculated, the point (X_1, Y_1) is plotted, and I is incremented by 1 to total the number of points that have been determined.

Since two points are needed to have a slope, I is tested to see if two or more points have been determined yet. If not, the program skips to line 15 where the first calculated Y value is stored in Z. In line 16, the first X value is stored in W. Then the program returns to line 5 where X is incremented by the initial value of D, to yield the second value of X.

Next, the second value of Y is calculated, the point (X_2,Y_2) is plotted, and 1 is added to I. Since two points have now been determined (I = 2), the test in line 10 causes the program to continue to line 11, where the first slope and first slope angle are determined.

Since three points (two plotted line segments) are needed to determine a change in slope, the test in line 12 senses that only two points have been determined, and jumps to line 14 where the first plot angle is stored in P. X_2 and Y_2 are then stored in W and Z, respectively, and the program again returns to line 5 where X_3 is computed. Then Y_3 is calculated, (X_3, Y_3) is plotted, I is incremented to a value of three, and in line 11 the plot angle from points (X_2, Y_2) and (X_3, Y_3) is computed.

Since there are three points plotted (two line segments and two plot angles), the value of change in plot angle may be calculated. The test in line 12 allows the program to continue to line 13 where the change in plot angle ($|P-Q|$) is computed as part of the △X calculation equation.

The program returns to line 5 where, for the first time, X is incremented by a calculated △X, rather than the initialized value of △X.

The program continues in this way until Y_i is found to exceed Y_{max} in line 9, and then the program stops.■

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Noniterative Digital Solution of Linear Transfer Functions

Bryan Finlay
Chief of Biomedical Engineering
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Introduction

This article will develop a technique for the precise, noniterative, digital solution of the time-domain response of linear transfer functions with constant coefficients. A computer program written in BASIC is provided for use on the Hewlett-Packard 9830A desktop computer. The program is suitable for solving equations that, in the Laplace domain, exhibit up to ten roots in either the numerator or denominator.

This program is shown to be at least ten times faster than certain iterative solutions when used for checking analog simulation data.

A complex second-order transfer function is used to demonstrate the use of the program in evaluating responses to impulse, step, ramp, and sinusoidal forcing functions.

Due to the availability of desktop computers it is thought that this relatively simple program could help to enhance educational courses in automatic control theory, as well as being of interest to personal computer users.

Most digital solutions of differential equations with constant coefficients involve iterative procedures. The efficient use of such procedures requires the operator to have a good knowledge of both the solution to the equations and the iterative procedure. A "feeling" for the time-course of the solution is particularly important when the response is oscillatory, otherwise an iterative solution can become quite inaccurate.

In the design and development of a complex automatic control system it is a common practice to use an analog computer simulation. The accuracy of the initial simulation is generally checked by comparing the analog results with those obtained from a digital solution of the equations. If the differential equations can be considered to have constant coefficients, then a noniterative solution of the time-domain response can be obtained by digital techniques.

Many automatic control theory problems present themselves in the form of the system transfer function and subsequent rearrangement to define the differential equations for iterative solution (as required by the Hewlett-Packard State Variables Pac). This can be a tedious, if not dissuading, process. It is the intention of this article to develop a technique that will permit the

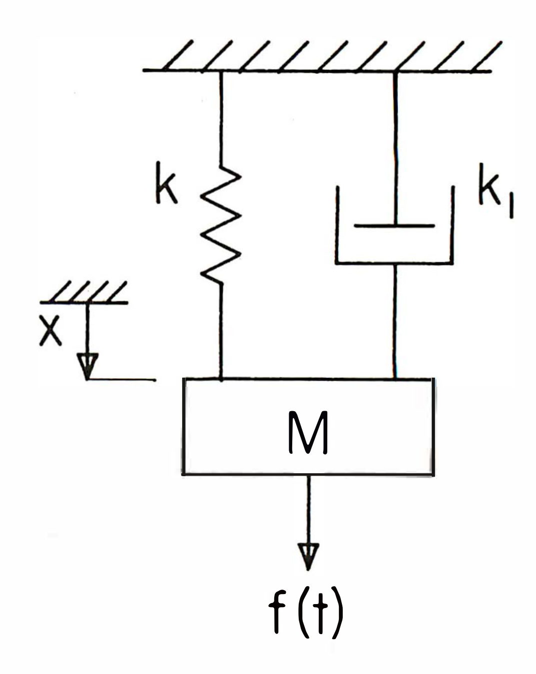


Figure 1: *Spring, mass, and damper model for a door-closing mechanism.*

digital solution of the time-domain response of linear transfer functions (or more generally Laplace transforms) by a noniterative process.

Analyzing the Response of Dynamic Systems

In order to emphasize the power of using transfer functions to analyze the response of dynamic systems, an example is given here to cover both the derivation and use of the transfer function. Consider a relatively massless object being moved by a spring and damper (dashpot) as shown in figure 1; this type of arrangement could characterize a door closing mechanism. An idealized spring exerts a force, f_s, that is directly proportional to the compression or extension, x, applied to it:

$$f_s = k x$$

An idealized damper exhibits Newtonian viscosity such that the force, f_d, that it exerts is directly proportional to the rate of compression or extension:

$$f_d = k_1 \frac{dx}{dt}$$

The constants of proportionality in these cases are k and k_1 and have units of N/m (lb/ft) and N per m/sec (lb per ft/sec) respectively.

Figure 2 shows the three forces acting on the mass and so permits us to apply Newton's second law of motion which tells us that "the summation of forces in a given direction is equal to the product of mass and acceleration that will take place in that direction."

$$f(t) - kx - k_1 \frac{dx}{dt} = M \frac{d^2x}{dt^2}$$

If the mass-acceleration term is small in relation to the other forces then this equation can be estimated as follows:

$$k_1 \frac{dx}{dt} + kx = f(t)$$

In the simplest case this equation can be solved by separation of variables and integration. However, the problem is compounded by the fact that the applied force $f(t)$ may be a time-dependent quantity itself. A few examples of such time-dependent functions are: impulse, step, ramp, or sine wave functions.

Virtually all automatic control systems contain elements that, in mathematical terms, require the use of differential equations. Consequently, aerospace, industrial, process-control and biological investigators have latched on to a convenient and consistent technique for solving these equations. The technique is summarized in the block diagram below:

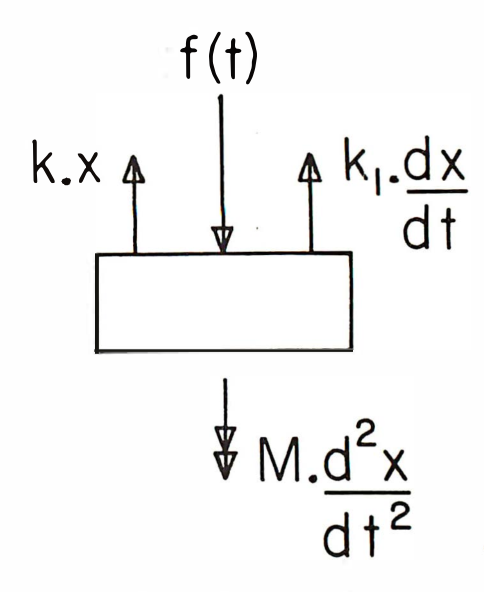


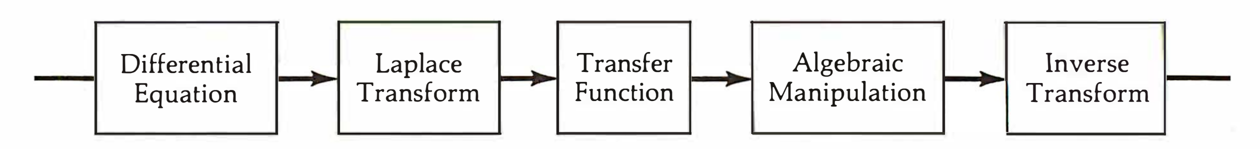
Figure 2: *Free-body diagram illustrating the total forces and the resultant mass-acceleration acting on the mass M of figure 1.*

Using standard tables each element in the differential equation is transformed to its Laplace transform. The transformed equation is rearranged to form the transfer function which is defined as the Laplace transform of the output divided by the Laplace transform of the input. In the example, if we consider the force $f(t)$ to be the input quantity and the displacement x to be the output then the transfer function is:

$$T(s) = \frac{X(s)}{F(s)} = \frac{1}{k_1 s + k} = \frac{1/k}{1 + \frac{k_1 s}{k}}$$

where $X(s)$ and $F(s)$ are the Laplace transforms of x and $f(t)$ respectively. The transfer function is a simple version of the Laplace transform since it assumes that all initial conditions are zero. This assumption effectively says that it does not matter whether the spring moves from 50 cm to 100 cm or moves from 150 cm to 200 cm; the resultant movement is 50 cm and the assumption of ideal springs means that the changes in forces will be the same. Note that it is the changes in forces from a steady state that will determine the dynamic behavior.

In the absence of a computer, the normal procedure to follow from this stage would be to choose an input quantity $f(t)$ and substitute its Laplace transform, $F(s)$, into the transfer function. The transfer function could then be manipulated algebraically by separating it into partial fractions to produce standard forms that may be found in a table of Laplace transforms. This set of standard equations in the Laplace domain could then be retransformed back to the time domain. For those seeking a more complete approach with detailed examples the Thaler and Brown textbook will provide good reading. The major



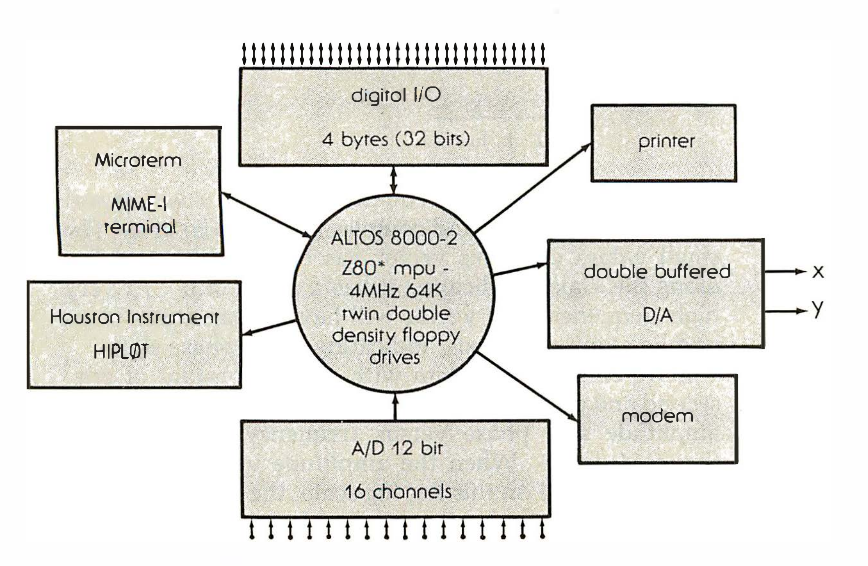
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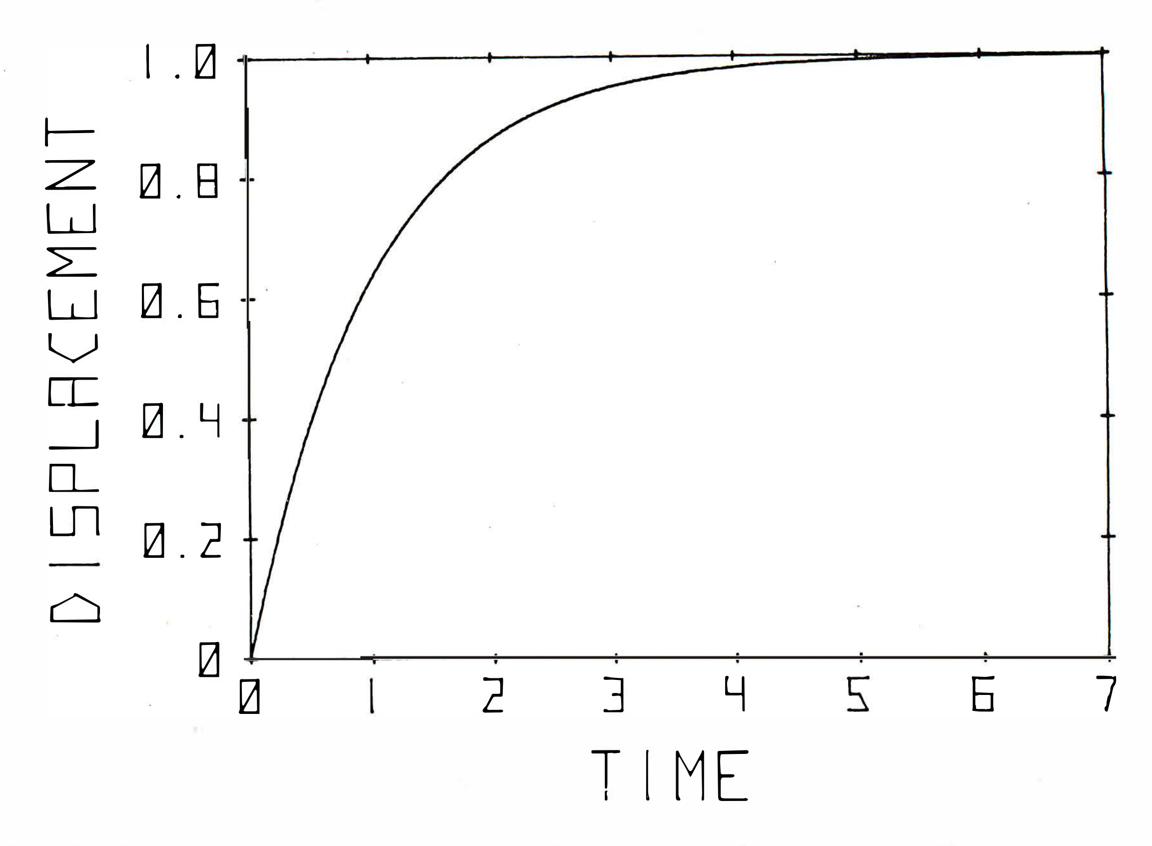


Figure 3: *Time-domain response of system in figure 1 when subjected to a step change in the force f(t).*

portion of this article provides a computer approach to the solution of the differential equations by means of the transfer function.

If the input, f(t), is a step change in force of unit value then the resulting value for $x(t)$ is given by:

$$x(t) = \frac{1}{k}\left(1 - e^{-t/\tau}\right)$$

where τ is a characteristic of the system and is defined as the time constant; in fact it is the ratio k_1/k. The displacement x will be 63.2% complete after a time $t = \tau$ and will be 98% complete when $t = 4\tau$. Consequently, the facility to read a time constant from a transfer function is valuable in describing the time-domain response of a system. A typical displacement response to a step change in force for a system with a one second time constant and stiffness k of unit magnitude is shown in figure 3.

High fidelity enthusiasts will know that the performance of a system is not clearly conveyed by its response to a step change in input. The frequency response provides a more informative set of data and concerns the response of a system to the input of a sine wave. Any linear system when subjected to a sine wave input will produce a sine wave of the same frequency at its output. However, the output sine wave will have an amplitude that is dependent upon the applied frequency. The peak of the output wave may also occur at a different time to that of the applied input. This phase shift, as it is called, is also frequency dependent.

A good high fidelity system will have a constant plot of amplitude versus frequency over its desired operating range, usually around 50 Hz to 20 kHz. In practice a voltage variation of 30% is considered to be good and would be expressed in logarithmic terms as a 3 dB variation.

The transfer function is an extremely powerful tool in the plotting of frequency response data since it can be shown mathematically that the substitution of $j\omega$ for s in the transfer function gives the amplitude and phase for a given frequency ω radians per second (note $\omega = 2\pi f$), after initial transients have decayed.

The operator j is used to indicate a vector at 90°. A vector a would lie on the x-axis of a graph and go from zero to a. The vector ja goes from zero to a on the y-axis of a graph. A vector jja would mean that the vector a had been rotated through 90° and 90° again, or 180°. This means that j^2a, as a vector, has the same meaning as $-a$. Consequently, the operator j can be looked upon mathematically as $\sqrt{-1}$ (note $j^2 = -1$).

Applying this knowledge to the transfer function for the spring and damper system yields:

$$T(j\omega) = \frac{1/k}{1 + j\omega\tau}$$

The denominator of this equation is a vector with a real part (x-axis) of unity and complex part (y-axis) of $\omega\tau$. For small values of ω this vector has a value of 1 and lies along the x-axis, indicating it has a phase of 0°. At very high frequencies the vector will have a magnitude of $\omega\tau$ and lie along the y-axis, indicating a 90° phase shift.

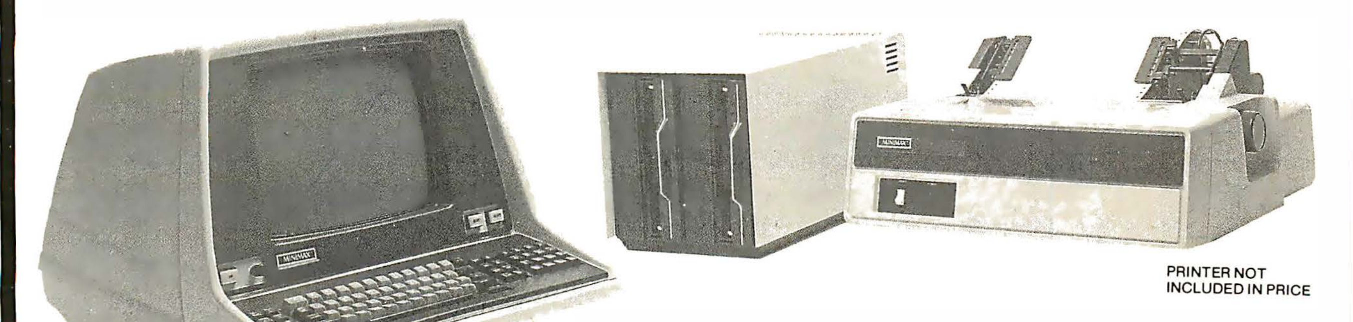
If we consider a system with a time constant of one second and unit stiffness of k then the resulting graphs of amplitude and phase versus frequency are shown in figures 4 and 5. When the amplitude versus frequency data are plotted on this log-log scale, the response is seen to approximate a horizontal low-frequency asymptote

Text continued on page 155; figures on pages 150-154

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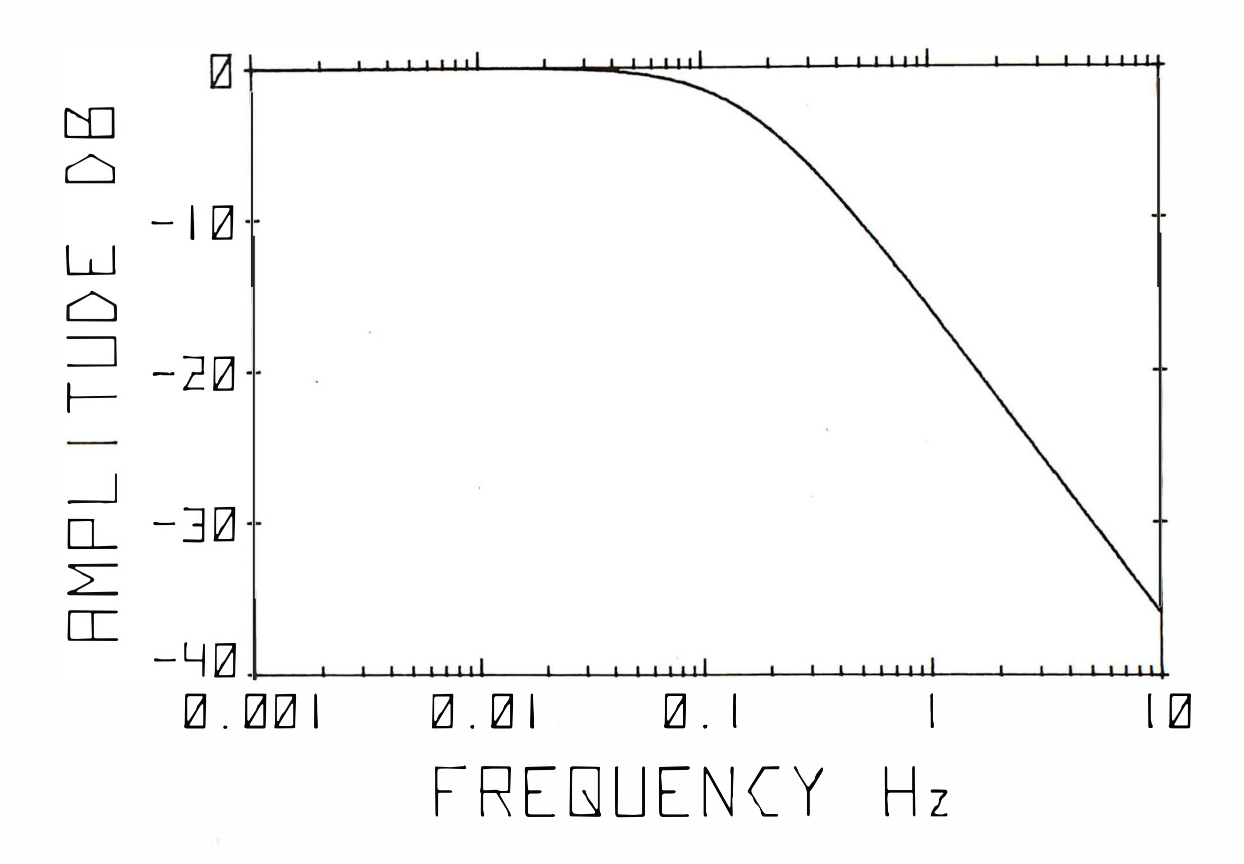


Figure 4: *Amplitude versus frequency data for the system in figure 1.*

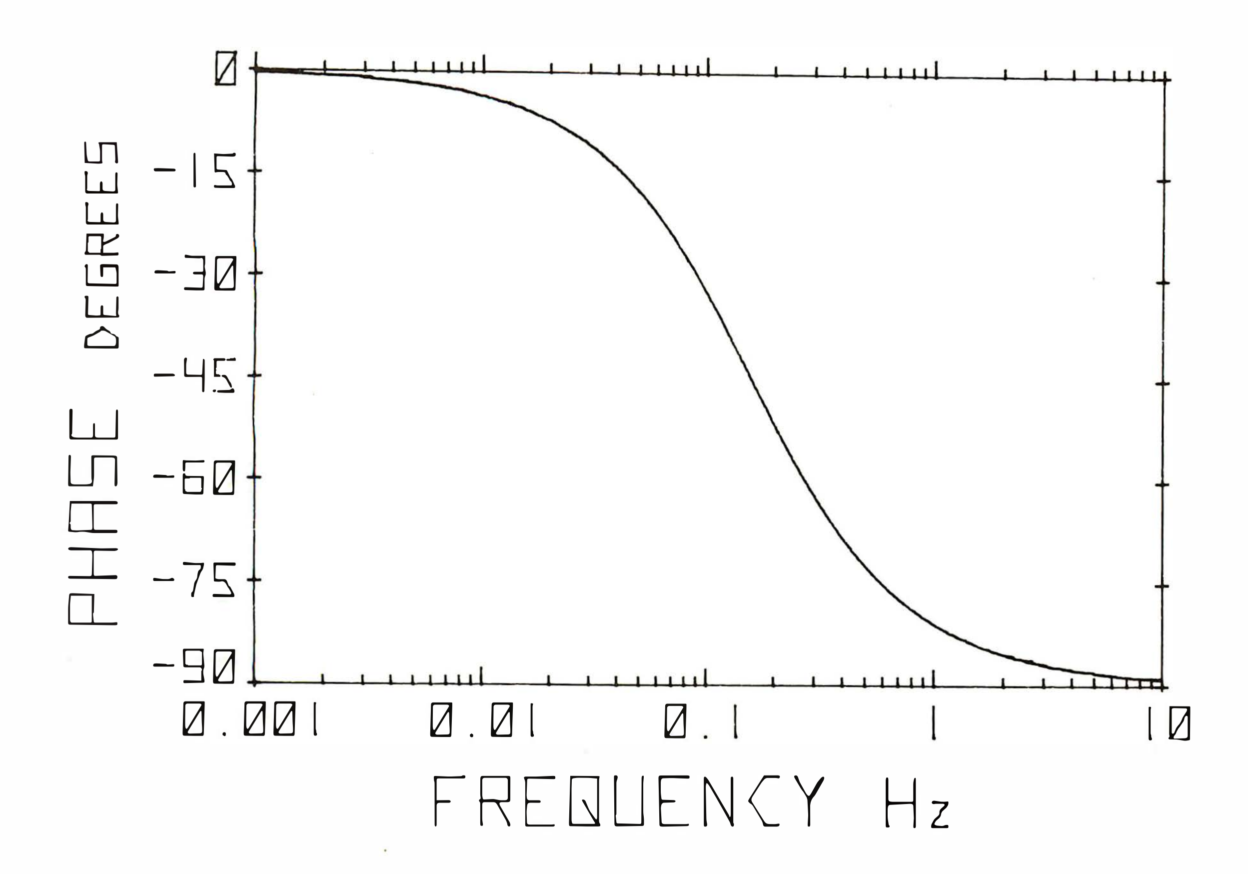
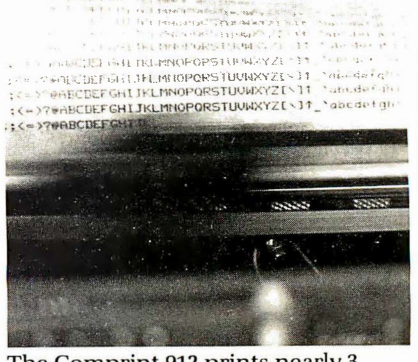


Figure 5: *Phase versus frequency data for the system in figure 1.*

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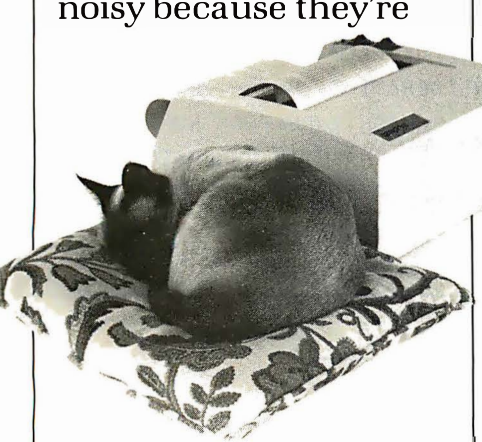
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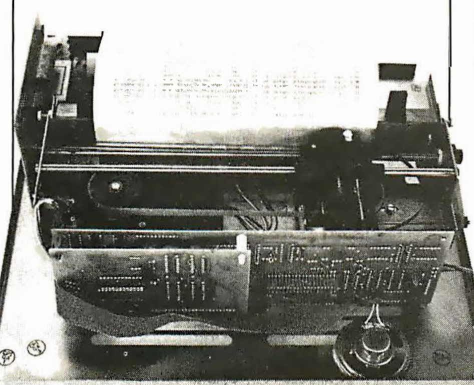


The Comprint 912 is quiet because it's electronic not mechanical.

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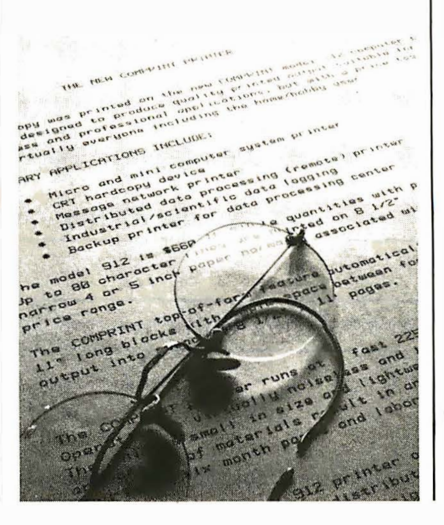
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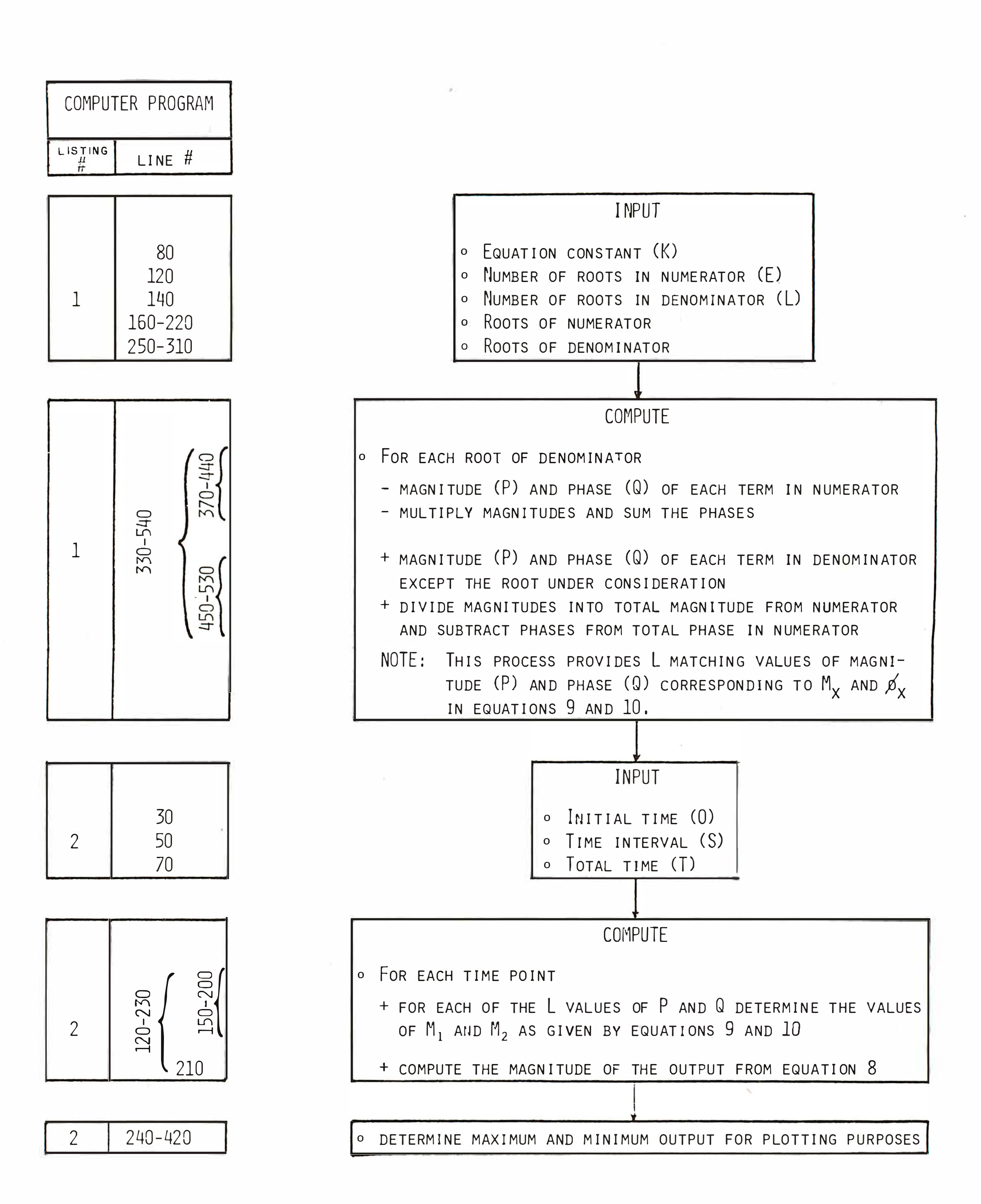


Figure 6: *Flow diagram and guide to the computer program which is provided in listing 1.*

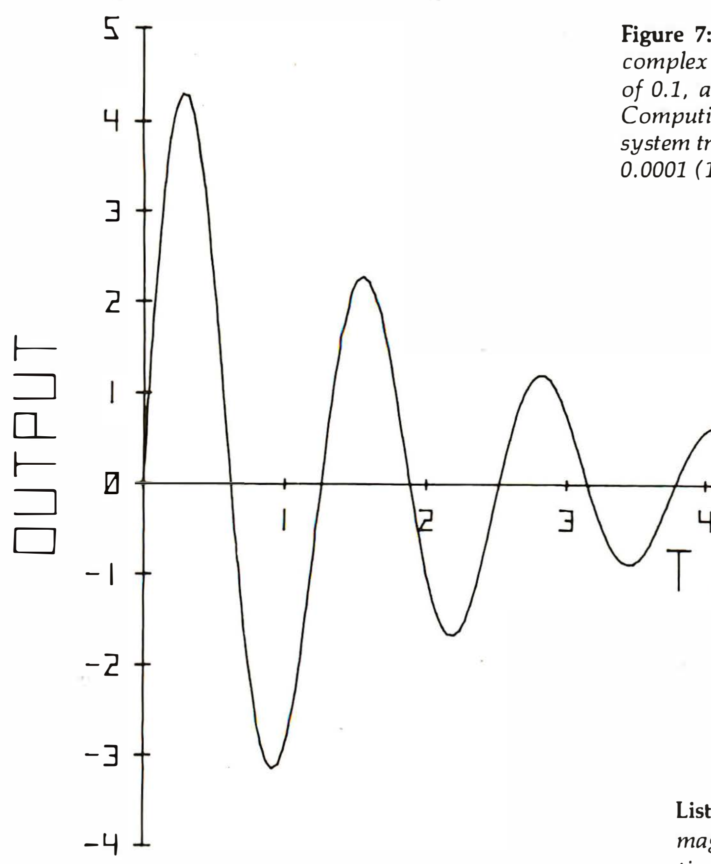


Figure 7: *Noniteratively computed unit impulse response of a complex second order lag with unity gain, damping factor (ζ) of 0.1, and natural angular frequency of 5 radians per second. Computing/plotting interval is 0.04. The equal real parts of the system transfer function have been made to differ by an amount 0.0001 (1 part in 5000).*

Text continued from page 148:
and a high-frequency asymptote with a slope of -20 dB/decade. The frequency at the point of intersection of these two asymptotes is 0.159 Hz in this example and, in general, is known as the break frequency and is given by:

$$\omega = \frac{1}{\tau} \quad \text{or} \quad f = \frac{1}{2\pi\tau}$$

It is at this frequency that the actual frequency response curve is 3 dB below the break point.

This simple example illustrates the use of transfer functions and helps to relate the response of a system in both the time domain and the frequency domain. The transfer function, therefore, provides a ready starting point for obtaining either time-domain or frequency-domain solutions. Since the substitution of $j\omega$ for s in the transfer function permits easy computation of the frequency response, it would be nice if a computer program was readily available to obtain plots of the time-domain response from the transfer function. It is the intent of this article to develop and illustrate the use of such a program.

General Solution of Laplace Transforms

Given a general Laplace transform F(s) which is the ratio of two polynomials:

$$F(s) = \frac{P(s)}{Q(s)}$$

with the order of Q(s) equal to, or greater than, the order of P(s), then an inverse Laplace transform, may be

Listing 1: *BASIC listing of the program that will compute the magnitude and phase of each of the terms in the transfer function.*

```
10 DIM K,A[10],B[10],C[10],D[10],E1,L1,P[10],Q[10],Z$[201]
20 PRINT "TRANSIENT RESPONSE PLOT FROM TRANSFER FUNCTION"
30 PRINT
40 PRINT "EXPRESS T.F.THUS:-  K(S+A1+JB1)(S+A2+JB2)(S+...)"
50 PRINT "                     (S+C1+JD1)(S+C2+JD2)(S+...)"
60 PRINT
70 DISP "WHAT IS K";
80 INPUT K
90 PRINT "K=";K
100 DIM G1,H1,R1,I1[1]
110 DISP "HOW MANY ROOTS IN NUMERATOR";
120 INPUT E
130 DISP "HOW MANY ROOTS IN DENOMINATOR";
140 INPUT L
150 IF E=0 THEN 240
160 FOR G=1 TO E
170 DISP "WHAT IS A("G")";
180 INPUT A[G]
190 DISP "WHAT IS B("G")";
200 INPUT B[G]
210 PRINT "A("G")=";A[G],"B("G")=";B[G]
220 NEXT G
230 PRINT
240 IF L=0 THEN 330
250 FOR H=1 TO L
260 DISP "WHAT IS C("H")";
270 INPUT C[H]
280 DISP "WHAT IS D("H")";
290 INPUT D[H]
300 PRINT "C("H")=";C[H],"D("H")=";D[H]
310 NEXT H
320 PRINT
330 FOR G=1 TO L
340 P[G]=1
350 Q[G]=0
360 IF E=0 THEN 450
370 FOR H=1 TO E
380 M=SQR((A[H]-C[G])↑2+(B[H]-D[G])↑2)
390 N=ATN((B[H]-D[G])/(A[H]-C[G]))
400 IF (A[H]-C[G]) >= 0 THEN 420
410 N=N-PI
420 P[G]=P[G]*M
430 Q[G]=Q[G]+N
440 NEXT H
450 FOR R=1 TO L
460 IF R=G THEN 530
470 M=SQR((C[R]-C[G])↑2+(D[R]--D[G])↑2)
480 N=ATN((D[R]-D[G])/(C[R]-C[G]))
490 IF (C[R]-C[G]) >= 0 THEN 510
500 N=N-PI
510 P[G]=P[G]/M
520 Q[G]=Q[G]-N
530 NEXT R
540 NEXT G
550 END
```

evaluated to define the time-domain solution.

Inversion to the time domain may be accomplished by applying a partial fraction expansion and thus expanding F(s) to a sum of simpler expressions each of which may be found in tables of Laplace transforms (refer to W D Day's Tables of Laplace Transforms). This system is illustrated below for a relatively simple transform:

$$F(s) = \frac{4}{(s+2)\ (s+3)} = \frac{A_1}{(s+2)} + \frac{A_2}{(s+3)} \qquad (1)$$

$$\text{Giving } F(s) = \frac{4}{(s+2)} - \frac{4}{(s+3)} \qquad (2)$$

In equation 2, the value of A_1 has been derived by multiplying both sides of equation 1 by $(s+2)$ and letting $s=-2$. Similarly, A_2 was obtained by multiplying by $(s+3)$ and setting $s=-3$. More precisely:

$$A_1 = \left| F(s) \times (s+2) \right|_{s=-2}$$

and,

$$A_2 = \left| F(s) \times (s+3) \right|_{s=-3}$$

for a general transform with n different non-complex roots in the denominator, then:

$$A_x = \left| F(s) \times (s+r_x) \right|_{s=-r_x} \qquad (3)$$

where r_x is the xth root.

The time-domain solution of equation 1 is:

$$f(t) = A_1 e^{-2t} + A_{2e}^{-3t}$$

or more generally:

$$f(t) = A_1 e^{-r_1 t} + A_2 e^{-r_2 t} + \ .\ .\ .\ .\ A_n e^{-r_n t} \qquad (4)$$

for a transform with n different non-complex roots in the denominator.

Combining equations 3 and 4, the general time-domain solution for a transform with n different non-complex roots is given by:

(5)

$$F(t) = \sum_{s=-r_1}^{-r_n} \left| (s+r_x) \times F(s) \times e^{st} \right|_{s=-r_x}$$

where x is assigned each value from 1 to n. This form of solution is generally referred to as the Residue Theorem solution (refer to the Thaler and Brown text for details). Equation 5 clearly lends itself to digital programming. However, when equal or repeated roots exist in the

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Figure 8: *Computed unit step response for the transfer function in figure 7. Computing/plotting interval is 0.04.*



denominator of F(s), the inverse transform of all the terms due to the repeated root, r_x, may be found as follows:

$$f(t) = \frac{1}{(m-1)!} \left| \frac{d^{m-1}}{ds^{m-1}} \{ (s+r_x) \times F(s) \times e^{st} \} \right|_{s=-r_x} \qquad (6)$$

where m is the number of times the root appears (for example: $m=2$ for two equal roots).

Listing 2: *This is a listing of the program designed to compute the total response, M, of a system as given in equation 8.*

```
10 DIM K,A[10],B[10],C[10],D[10],E1,L1,P[10],Q[10],Z3[201]
20 DISP "WHAT IS INITIAL TIME T(0)";
30 INPUT O
40 DISP "WHAT IS TIME INTERVAL DT";
50 INPUT S
60 DISP "TOTAL TIME - MAX=T(0)+200*DT";
70 INPUT T
80 PRINT "INITIAL TIME=";O
90 PRINT "TIME INTERVAL=";S
100 PRINT "FINAL TIME=";T
110 PRINT
120 FOR U=O TO T STEP S
130 V=W=0
140 H=1+INT((U-O)/S)
150 FOR G=1 TO L
160 X=P[G]*EXP(-C[G]*U)
170 Y=Q[G]-D[G]*U
180 V=V+X*COS(Y)
190 W=W+X*SIN(Y)
200 NEXT G
210 Z[H]=K*SGN(V)*SQR(V↑2+W↑2)
220 DISP "COMPUTING"
230 NEXT U
```

Listing 2 continued on page 160

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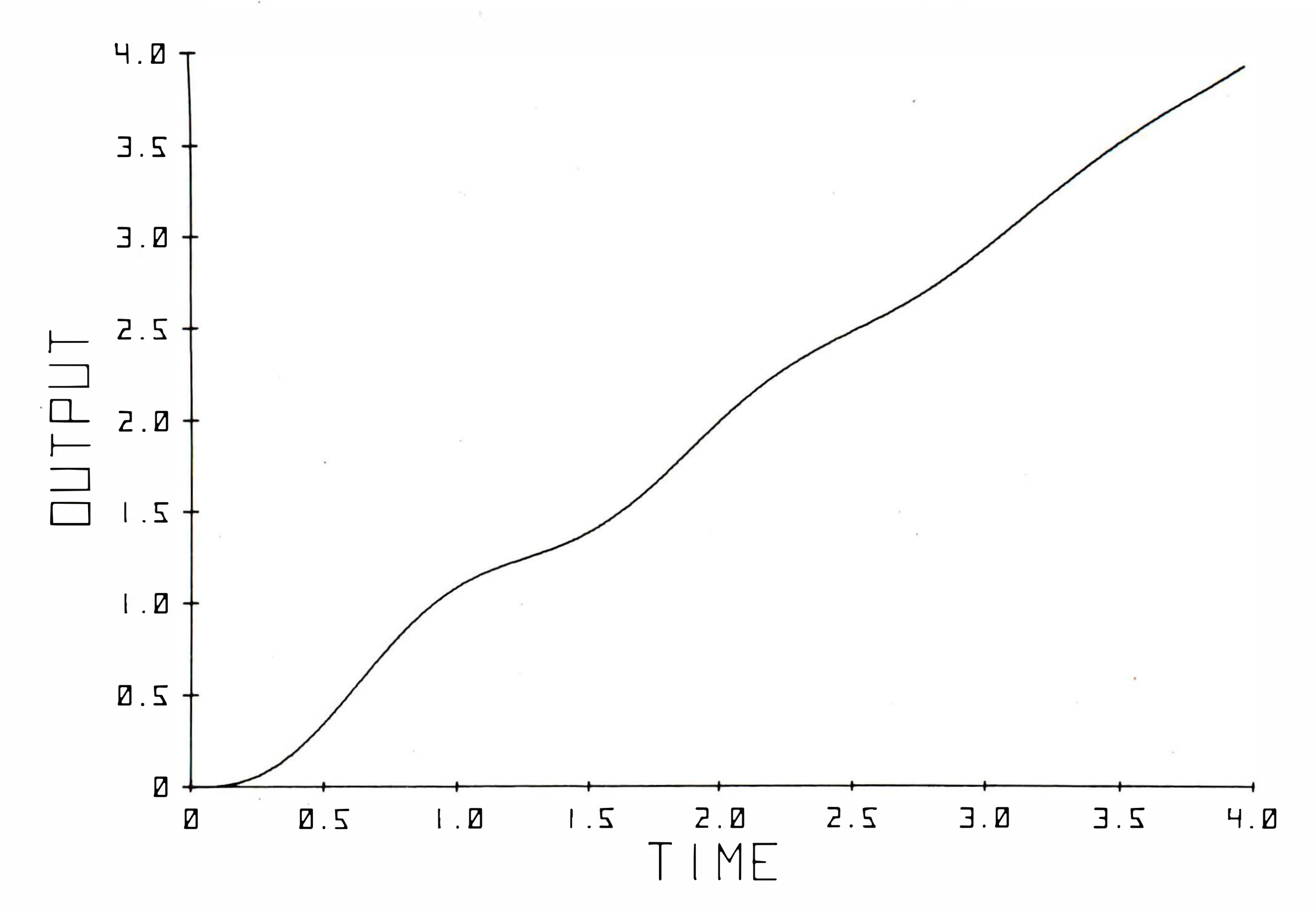


Figure 9: *Unit ramp response computed for the transfer function in figure 7. Computing/plotting interval is 0.02. The equal real parts of the transfer function of the unit ramp have been set to differ by an amount 1 × 10^{-8}.*

Listing 2 continued:

```
240 DISP "INPUT MAX & MIN (0=YES 1=AUTO)";
250 INPUT I
260 IF I=1 THEN 320
270 DISP "MAX OUTPUT";
280 INPUT M
290 DISP "MIN OUTPUT";
300 INPUT N
310 GOTO 430
320 M=N=Z[1]
330 FOR U=0 TO T STEP S
340 H=1+(U-0)/S
350 IF Z[H]<M THEN 380
360 M=Z[H]
370 GOTO 400
380 IF Z[H]>N THEN 400
390 N=Z[H]
400 NEXT U
410 IF N<0 THEN 430
420 N=0
430 END
```

Solution by Residue Theorem

Digital programming of the differentiation of equation 6 is not the simplest process and, in practice, is unnecessary. Due to the number crunching capacity of small-scale desktop digital computers, the problem of two equal roots can be surmounted quite readily. When inputting the data on the roots, one of the two equal roots is changed by a relatively small amount (approximately 0.1 or 1%). While electronic control systems may employ components with tolerances causing a 1% error in the roots, experience tells us that the difference in the plotted curves will be virtually indistinguishable in any practical system.

The problem of repeated roots has effectively been solved, and it is necessary only to develop equation 5 to a form capable of handling complex roots.

If r_x is complex (of the form: $-a-jb$), then equation 5 tells us that the root r_x makes a contribution, $f_1(t)$, to the total response in the time domain at time t where:

$$f_1(t) = \left| (s+a+jb) \times F(s) \times e^{st} \right|_{s=-a-jb}$$

giving: $f_1(t) = M_x e^{j\phi} e^{-[a+jb]t}$

or rearranging: $f_1(t) = M_x e^{-at} e^{j[\phi-bt]}$ (7)

The real (Re) and imaginary (Im) parts of $f_1(t)$ are respectively:

$$f_1(t)\ (\text{Re}) = M_x e^{-at} \cos(\phi-bt)$$
$$f_1(t)\ (\text{Im}) = M_x e^{-at} \sin(\phi-bt)$$

The total system response, M, at a specific time t is given by:

$$M = \sqrt{M_1^2 + M_2^2} \quad (8)$$

$$\text{Where } M_1 = \sum_{x=1}^{n} M_x e^{-r_x t} \cos(\phi_x - b_x t) \quad (9)$$

$$\text{and } M_2 = \sum_{x=1}^{n} M_x e^{-r_x t} \sin(\phi_x - b_x t) \quad (10)$$

Computer Program

The BASIC program developed for solving these equations is shown in listing 1. F(*s*) is assumed to have a maximum tenth-order numerator and/or denominator of the general form:

$$F(s) = \frac{K(s+A1+jB1)\,(s+A2+jB2)\,\ldots\ldots\,(s+A10+jB10)}{(s+C1+jD1)\,(s+C2+jD2)\,\ldots\ldots\,(s+C10+jD10)}$$

Obviously, any complex root must have a conjugate for the equation to have any meaning.

The flow diagram for the solution of the equations is given in figure 6. The program permits 201 output data points to be evaluated, or 200 time divisions. Full four-word accuracy is employed in the intermediate computations and, to save memory, two-word accuracy is employed in the stored values of the output.

In practice, three types of output have been found useful:

- A tabular printout of time and magnitude.
- A thermal printer plot of output versus time provides crude but rapid viewing of the unknown response and so permits optimizing the time interval and total time to achieve the most informative plot.
- A digital, pen-plotted output for formal presentation.

Use of link statements on the HP9830A allowed this program to be run with 2 K words of memory. However, a 4 K word memory permitted simultaneous loading of all program files onto the key files.

Results and Discussion

Consider the complex second-order transfer function with unity gain, damping factor (ζ) of 0.1, and natural angular frequency of 5 radians per second:

$$\frac{V_o(s)}{V_i(s)} = \frac{25}{s^2+s+25} \qquad (11)$$

For a unit impulse, $v_i(t)$, then $V_i(s) = 1$ and:

$$V_o(s) = F(s) = \frac{25}{(s+0.5+j4.975)\,(s+0.5-j4.975)}$$

Since the computer interprets the real parts of these roots as being equal, it is necessary to change one of them by a small amount (approximately 0.5001 in this case).

The impulse response of equation 11 is shown in figure 7. This curve was computed for 201 points from $t=0$ to 8 at 0.04 intervals.

Frequently, a digital computer solution is required as a check on the accuracy of an analog computer simulation. The efficiency of this computer program in providing such data is illustrated in table 1. The test is to compute the output at 0.5-second intervals for the first 5 seconds of figure 7. The performance of the program was compared with a standard iterative procedure employed by the Hewlett-Packard Math Pac volume 1.

Table 1: *A measure of the efficiency of the computer program in verifying the accuracy of an analog computer simulation.*

TIME (seconds)	OUTPUT				
	RESIDUE THEOREM	ITERATIVE SOLUTION Integration Time (seconds)			
		0.5	0.1	0.01	0.005
0	0.000	0.000	0.000	0.000	0.001
0.5	2.381	9.375	2.054	2.378	2.380
1.0	-2.943	-43.36	-2.757	-2.940	-2.943
1.5	2.194	117.8	2.433	2.195	2.194
2.0	-0.9269	-161.9	-1.564	-0.9322	-0.9281
2.5	-0.1850	-290.8	0.5962	-0.1778	-0.1834
3.0	0.7909	2775	0.1653	0.7850	0.7895
3.5	-0.8654	-10265	-0.5901	-0.8630	-0.8648
4.0	0.5901	22981	0.6902	0.5914	0.5903
4.5	-0.2045	-15666	-0.5620	-0.2083	-0.2053
5.0	-0.1051	-130420	0.3283	-0.1010	-0.1042
Total Time for Computation and Printout (seconds)	25	10	25	200	390

It is clear from table 1 that the cumulative errors for an iterative process with integration time, δt, of 0.1 produced inadequate results at $t=5$. Accuracies of 4% and 1% are obtained at $t=5$, for integration times of 0.01 and 0.005 seconds respectively. However, the total computing times of 200 and 390 seconds respectively are drastically larger than the 25 seconds associated with the Residue Theorem approach. By employing fast memory in the HP 9830A the total computing and printout time can be reduced to 15 seconds. Use of the Infotek FP 30, fast processor, can reduce this total time even further to approximately 8 seconds.

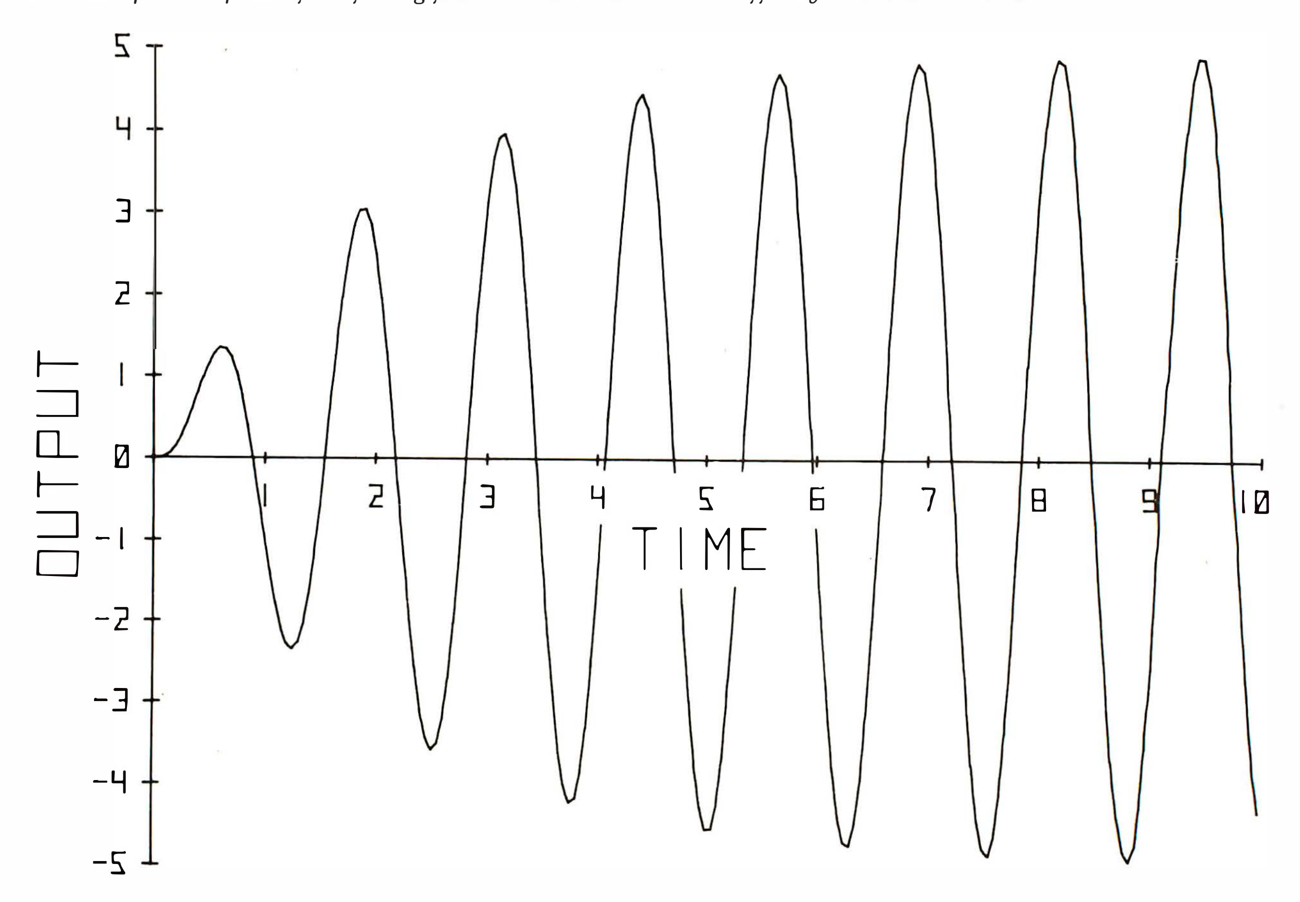
A unit step input (ie: $V_i(s)=s^{-1}$) in equation 11 gives F(s) as:

$$F(s)=\frac{25}{(s+0+j0)\ (s+0.5001+j4.975)\ (s+0.5-j4.975)} \quad (12)$$

A unit ramp input (ie: $V_i(s) = s^{-2}$) in equation 11 gives F(s) as:

$$F(s) = \frac{25}{(s+0+j0)(s+1\times10^{-8}+j0)(s+0.5001+j4.975)(s+0.5-j4.975)} \quad (13)$$

Figure 10: *Computed initial transients of the transfer function used in figure 7, when it is subjected to a unit sinusoidal forcing function of the same frequency (five radians per second) as the natural frequency of the system under test. Computing/plotting interval is 0.05. The equal real parts of the forcing function have been made to differ by an amount 1 × 10⁻⁸.*



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Figure 11: *Computed transient response of the transfer function used in figure 7, when subjected to a unit sinusoidal forcing function of ten radians per second, or twice the natural frequency of the system in question. While the computing/plotting interval of 0.05 is too large to give a smooth curve, the noniterative solution ensures that all points plotted lie on the "true" response curve.*

and the real part of the repeated root ($s=0$) has been made negligible (1×10^{-8}) in relation to the other roots. Due to the 12-point accuracy employed by the HP9830A, roots smaller than 1×10^{-8} should not be used when handling trigonometric functions such as arctangent. Similarly, any two roots must have a difference that is greater than 1×10^{-8}. While equation 13 may be solved using a value of 1×10^{-10} for the root at $s=0$, the accuracy decreases rapidly, and the solution becomes meaningless with a value of 1×10^{-12}. However, a root of 1×10^{-8} would represent a time constant of 3.17 years. If, for any reason, the time constants are in the order of months or years, then the whole problem should be time-scaled before programming.

The solutions to equations 12 and 13 are plotted in figures 8 and 9 respectively.

In educational environments, these digital simulations help emphasize the transient behavior of systems subjected to sinusoidal forcing functions, without the possibility of causing a system overload. Figure 10 illustrates the effect of inputting equation 11 with a unit sine wave

$$v_i(t) = \sin(wt) \quad V_i(s) = \frac{w}{s^2+w^2}$$

with a frequency of 5 radians per second, that being equal to the natural frequency of the system. Since $\zeta=0.1$, this is almost the resonant frequency.

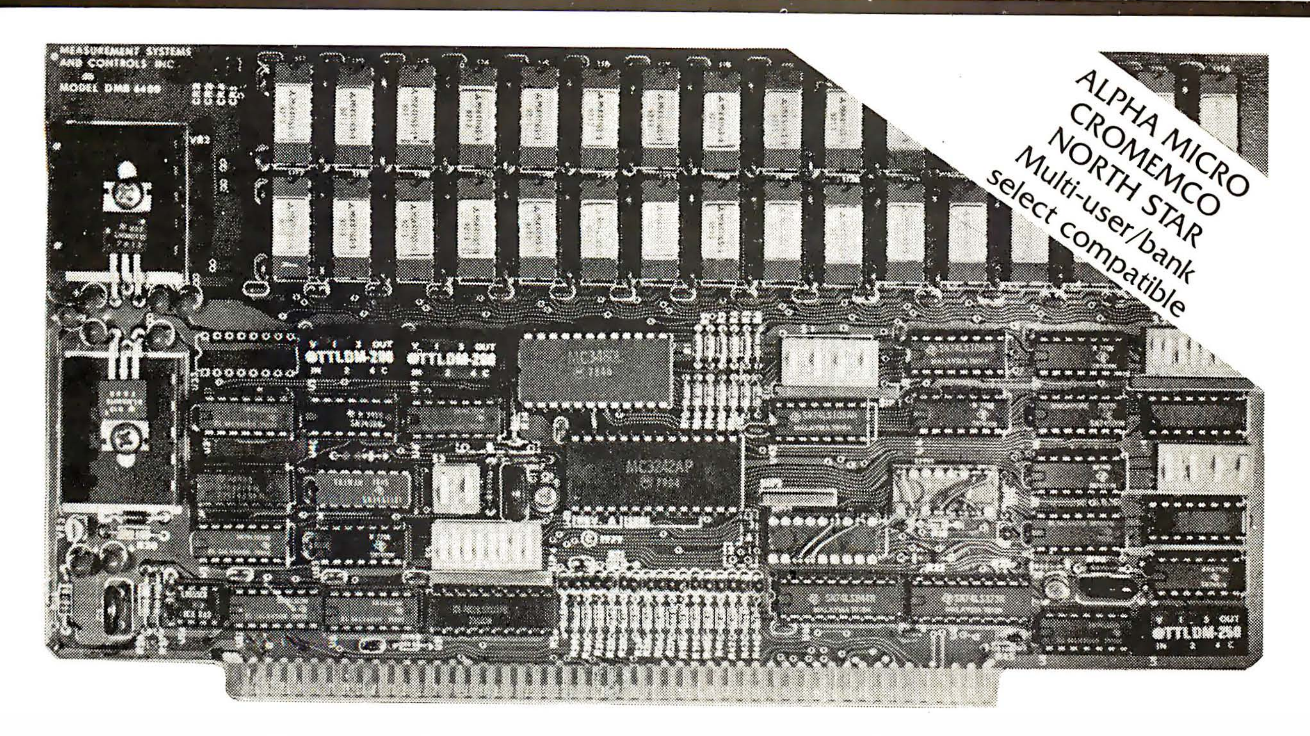
Figure 11 illustrates the effect of inputting equation 11 with a unit, 10 radians per second sine wave, which is twice the natural frequency of the system.

While the axis labels in figures 7 thru 10 are most convenient for the presentation of those results, the printout employed in figure 11 is more versatile when a great number of amplitudes and time scales are expected. ■

REFERENCES

Day W D, Tables of Laplace Transforms, London: Iliffe, 1966.

Thaler G J and Brown R G, *Analysis and Design of Feedback Control Systems*, New York, McGraw-Hill, 1960, pages 9-29.



Model DMB-6400 Series dynamic 64k byte RAMS incorporate the features which are standard in the DM-6400 Series and adds bank select for multi-user-timesharing applications.

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Listing 1 continued from page 85:

```
                        ;ROUTINE LINE
                        ;       GENERATE THE LINE FROM THE CURRENT CURSOR
                        ;          POSITION TO THE POINT X,Y IN H,L.
                        ;       USES DOT TO ACTUALLY DISPLAY THE POINTS.
                        ;
                        ;BLOCK 1:   PRELIMINARIES
                        ;
                        ;   1.1--SECTOR DETERMINATION
                        ;
01F1 F5         LINE:   PUSH    PSW     ;SAVE THE WORLD
01F2 C5                 PUSH    B       ;   NOTE: ORDER IS SET BY
01F3 D5                 PUSH    D       ;   RESTORE IN DOT
01F4 E5                 PUSH    H       ;
01F5 CD6401             CALL    CU000   ;COORDINATES NEED CHANGING
01F8 3AAD04             LDA     XPOS    ;GET CURRENT CURSOR POSITION
01FB BC                 CMP     H       ;WHICH IS BIGGER?
01FC DA0502             JC      L100    ;XF
01FF 94                 SUB     H       ;NEED A-H
0200 0600               MVI     B,00H   ;SET SECTOR CODE TO ZERO
0202 C30A02             JMP     L101    ;AND CONTINUE
0205 2F         L100:   CMA             ;NEED H-A
0206 3C                 INR     A       ;  WHICH REQUIRES 2'S COMP
0207 54                 ADD     H       ;  AND AN ADD
0208 0604               MVI     B,04H   ;SECTOR CODE GETS 4
020A 57         L101:   MOV     D,A     ;XP GOES IN D
020B 3AAC04             LDA     YPOS    ;DO THE SAME FOR Y
020E BD                 CMP     L       ;WHICH IS LARGER
020F DA1702             JC      L102    ;YF IS
0212 95                 SUB     L       ;YC IS
0213 5F                 MOV     E,A     ;SAVE IT
0214 C31F02             JMP     L103    ;AND CONTINUE
0217 2F         L102:   CMA             ;AGAIN, GET 2'S COMPLIMENT
0218 3C                 INR     A       ;
0219 85                 ADD     L       ;  TO FIND YF-YC
021A 5F                 MOV     E,A     ;  AND SAVE IT
021B 3E02               MVI     A,02H   ;INCR SECTOR CODE BY 2
021D 80                 ADD     B       ;
021E 47                 MOV     B,A     ;NEW SECTOR VALUE
021F 7A         L103:   MOV     A,D     ;IS XP < YP?
0220 BB                 CMP     E       ;IF SO THEY NEED EXCHANGING
0221 D22702             JNC     L104    ;  OK AS THEY ARE
0224 53                 MOV     D,E     ;XP = YP
0225 5F                 MOV     E,A     ;  AND YP = OLD XP
0226 04                 INR     B       ;AND SECTOR CODE GETS ONE MORE
                        ;
                        ;   1.2--PARAMETER INITIALIZATION
                        ;
0227 2E00       L104:   MVI     L,00H   ;XT = 0
0229 62                 MOV     H,D     ;XP
022A E5                 PUSH    H       ;XP, XT
022B 65                 MOV     H,L     ;0,0
022C E5                 PUSH    H       ;TA = 0
022D 6B                 MOV     L,E     ;H,L = YP
022E 22A104             SHLD    DY      ;DY = +YP
0231 7A                 MOV     A,D     ;DETERMINE DX
0232 2F                 CMA             ;  WHICH IS 2'S COMPLIMENT
0233 6F                 MOV     L,A     ;  OF XP
0234 26FF               MVI     H,0FFH  ;  I.E. DX = -XP
0236 23                 INX     H       ;
0237 22A304             SHLD    DX      ;SAVE FOR LOOOP
023A 37                 STC             ;T0 = 1/2 DX
023B 7C                 MOV     A,H     ;ARITH SHIFT RIGHT
023C 1F                 RAR             ;  OF H,L
023D 67                 MOV     H,A     ;HIGH  BYTE DONE
023E 7D                 MOV     A,L     ;NOW DO LOW BYTE
023F 1F                 RAR             ;
0240 6F                 MOV     L,A     ;ALL DONE
0241 E5                 PUSH    H       ;SAVE T0
                        ;
                        ;   1.3--SET UP COORDINATE TRANSFORMATION TABLE
                        ;
0242 21BD03             LXI     H,MXT   ;CALCULATE CORRECT MOVES
0245 78                 MOV     A,B     ;OFFSET INTO TABLE
0246 07                 RLC             ;EACH ENTRY IS FOUR BYTES
0247 07                 RLC             ;
0248 5F                 MOV     E,A     ;ADD TO BASE ADDRESS
0249 1600               MVI     D,0
024B 19                 DAD     D       ;H,L IS NOW ADDRESS OF M0X
024C 5E                 MOV     E,M     ;GET M0X
024D 23                 INX     H       ;AIM AT M0Y
024E 56                 MOV     D,M     ;AND GET IT TOO
024F EB                 XCHG            ;SHIFT TO H,L
0250 22A504             SHLD    M0X     ;AND STORE IN MOVE ZERO
0253 EB                 XCHG            ;NOW GET 'ONE' MOVE
0254 23                 INX     H       ;WHICH ARE THE NEXT 2 ENTRIES
0255 5E                 MOV     E,M     ;M1X
0256 23                 INX     H       ;
0257 56                 MOV     D,M     ;M1Y
0258 EB                 XCHG            ;GET SET
0259 22A704             SHLD    M1X     ;  AND STORE
                        ;
                        ;BLOCK #2:   THE ACTUAL LINE GENERATION LOOP
                        ;
                        ;   2.1--DISPLAY THE CURRENT POINT
                        ;
025C CD7701     L200:   CALL    DOT     ;DISPLAY THE CURRENT POINT
                        ;
                        ;   2.2--TEST FOR DONE
                        ;
025F C1                 POP     B       ;B,C=T0
0260 D1                 POP     D       ;D,E = TA
0261 E1                 POP     H       ;H,L = XP, XT
0262 7D                 MOV     A,L     ;XT
0263 BC                 CMP     H       ;XP
0264 D2EC01             JNC     D402    ;ALL DONE, GO RESTORE
0267 2C                 INR     L       ;XT = XT + 1
0268 E5                 PUSH    H       ;SAVE FOR NEXT ITERATION
                        ;
                        ;   2.3--DETERMINE NEXT MOVE
                        ;
0269 2AA104             LHLD    DY      ;GET DY
026C 19                 DAD     D       ;TA = TA + DY
026D E5                 PUSH    H       ;SAVE FOR NEXT ITERATION
026E 09                 DAD     B       ;TA + T0
026F DA7902             JC      L240    ;IF POSITIVE
                        ;
                        ;   2.4--MAKE THE REQUIRED MOVE
                        ;
```

Listing 1 continued on page 170

Circle 47 on inquiry card.

Listing 1 continued:

```
0272 C5        L242:  PUSH   B        ;T0 UNCHANGED WITH MOVE ZERO
0273 2AA504           LHLD   M0X      ;M0X IN L; M0Y IN H
0276 C38102           JMP    L241     ;  GO MOVE
0279 2AA304    L240:  LHLD   DX       ;MOVE ONE INCREMENTS T0
027C 09               DAD    B        ;T0 = T0 + DX
027D E5               PUSH   H        ;SAVE FOR NEXT ITERATION
027E 2AA704           LHLD   MIX      ;MIX IN L; MIY IN H
0281 EB        L241:  XCHG            ;MAKE ROOM FOR AN ADDRESS
0282 21AC04           LXI    H,YPOS   ;UPDATE Y FIRST
0285 7A               MOV    A,D      ;M?Y
0286 86               ADD    M        ;  IS ADDED TO YPOS
0287 77               MOV    M,A      ;NEW YPOS
0288 23               INX    H        ;DO THE SAME FOR XPOS
0289 7B               MOV    A,E      ;
028A 86               ADD    M        ;
028B 77               MOV    M,A      ;
028C C35C02           JMP    L200     ;END OF LINE GENERATION LOOP
               ;
               ;ROUTINE CHAR
               ;      GENERATE THE ASCI CHARACTER IN REGISTER A.
               ;      CHARACTERS ARE BASED ON A VARIABLE WIDTH
               ;         4 BY 5 MATRIX.
               ;      THE CURSOR DEFINES THE LOWER LEFT CORNER
               ;         OF THE DOT MATRIX.
               ;      CURSOR IS MOVED TO THE NEXT CHARACTER POSITION.
               ;      LOWER CASE IS CONVERTED TO UPPER CASE.
               ;      PARITY IS IGNORED.
               ;      THE FOLLOWING CONTROL CHARACTERS ARE RECOGNIZED:
               ;MNEMONIC ASCII HEX     FUNCTION
               ;MAXR     NUL   00      DISPLAY MODE - 128 BY 128 COLOR
               ;MAXC     SOH   01      DISPLAY MODE - 64 BY 64 COLOR
               ;R128     STX   02      DISPLAY MODE - 128 BY 128 COLOR
               ;R4     ETX     03     DISPLAY MODE - 64 BY 64 COLOR
               ;
               ;BS       BS    08      BACKSPACE:  XPOS=XPOS-6
               ;HT       HT    09      HOR. TAB:  XPOS=(XPOS+32)MOD 32
               ;LF       LF    0A      LINE FEED:  YPOS=YPOS-8
               ;VT       VT    0B      VERT. TAB:  YPOS=((YPOS-32) MOD
32)-6
               ;FF       FF    0C      FORM FEED:  XPOS=0, YPOS=MAX-6
               ;CR       CR    0D      CAR. RET.:  XPOS=0
               ;
               ;BLK      DLE   10      BLACK (ERASE)
               ;RED      DC1   11      RED
               ;BLU      DC2   12      BLUE
               ;MAG      DC3   13      MAGENTA
               ;GRN      DC4   14      GREEN
               ;YEL      NAK   15      YELLOW
               ;CYN      SYN   16      CYAN
               ;WHI      ETB   17      WHITE
               ;
               ;
               ;BLOCK 1:  CHARACTER TYPE DETERMINATION
               ;
028F F5        CHAR:  PUSH   PSW      ;SAVE THE WORLD
0290 C5               PUSH   B        ;NOTE: ORDER IS SET BY
0291 D5               PUSH   D        ;   RESTORE IN DOT
0292 E5               PUSH   H        ;
0293 01EC01           LXI    B,D402   ;FAKE A CALL FROM THE
0296 C5               PUSH   B        ;  REGISTER RESTORE SEQUENCE
0297 E67F             ANI    7FH      ;CLEAR PARITY BIT
0299 FE20             CPI    20H      ;COMPARE TO A BLANK
029B DA1C03           JC     C500     ;  CONTROL CHARACTER
029E FE60             CPI    60H      ;COMPARE TO ACCENT GRAVE
02A0 DAA502           JC     C100     ;  UPPER CASE
02A3 E65F             ANI    5FH      ;CONVERT LOWER CASE TO UPPER
02A5 2AAC04    C100:  LHLD   YPOS     ;GET CURRENT CURSOR POSITION
02A8 EB               XCHG            ;  BUT IN D,E
               ;
               ;BLOCK 2:  CALCULATE THE CHARACTER MATRIX ADDRESS
               ;      A = ASCII CHARACTER      D,E = XPOS, YPOS
               ;
02A9 21DD03           LXI    H,CHRX   ;BASE ADDRESS OF CHAR TABLE
02AC D620             SUI    20H      ;ZEROTH ENTRY IN TABLE IS BLANK
02AE 4F               MOV    C,A      ;3 BYTES PER ENTRY
02AF 0600             MVI    B,00H    ;  SO MULTIPLY OFFSET BY3
02B1 09               DAD    B        ;ONCE
02B2 09               DAD    B        ;  TWICE
02B3 09               DAD    B        ;    THRICE
02B4 7E               MOV    A,M      ;GET BYTE 0 WITH FLAGS
02B5 E603             ANI    03H      ;ISOLATE WIDTH FIELD
02B7 FE03             CPI    03H      ;FIVE WIDE?
02B9 CCF302           CZ     C400     ;YES, TAKE CARE OF IT
02BC 42               MOV    B,D      ;SAVE STARTING XPOS
02BD C603             ADI    03H      ;WIDTH OF CHAR + 1
02BF 82               ADD    D        ;XPOS OF NEXT CHARACTER
02C0 57               MOV    D,A      ;D,E IS NEXT CHAR POSITION
02C1 D5               PUSH   D        ;SAVE UNTIL DONE
02C2 50               MOV    D,B      ;RESTORE CURRENT POSITION
02C3 7E               MOV    A,M      ;ONE LAST FLAG TO TEST
02C4 07               RLC             ;IS THIS A DESCENDING CHAR
02C5 D2CA02           JNC    C300     ;  NO.  GO GENERATE IT
02C8 1D               DCR    E        ;  YES.  DOWN TWO ON Y
02C9 1D               DCR    E        ;
               ;
               ;BLOCK 3:  GENERATE THE ACTUAL CHARACTER
               ;      A = MASK FOR BOTTOM ROW
               ;      D,E = XPOS, YPOS
               ;      H,L = ADDRESS OF FIRST BYTE OF CHAR TABLE ENTRY
               ;
02CA EB        C300:  XCHG            ;GET REGISTERS IN POSITION
02CB CDE102           CALL   C310     ;DO BOTTOM ROW OF CHAR
02CE CDDF02           CALL   C305     ;SECOND ROW
02D1 CDE102           CALL   C310     ;THIRD ROW
02D4 CDDF02           CALL   C305     ;FOURTH ROW
02D7 CDE102           CALL   C310     ;AND TOP ROW
02DA E1               POP    H        ;RETRIEVE PRECALCULATED CURSOR
02DB 22AC04           SHLD   YPOS     ;AND UPDATE CURSOR
02DE C9               RET             ;ALL DONE
02DF 13        C305:  INX    D        ;NEXT BYTE IN TABLE
02E0 1A               LDAX   D        ;  GOES IN A
02E1 0604      C310:  MVI    B,04H    ;COLUMNS PER ROW
02E3 E5               PUSH   H        ;SAVE STARTING POSITION
02E4 07        C311:  RLC             ;SHOULD POINT BE ON?
02E5 22AC04           SHLD   YPOS     ;UPDATE CURSOR
02E8 DC7701           CC     DOT      ;PUT UP THE POINT IF REQUIRED
02EB 24               INR    H        ;NEXT X
02EC 05               DCR    B        ;COUNT DOWN
```

Listing 1 continued on page 172

3rd Generation S-100: Chosen by Professionals, Supported by CompuPro™

Why S-100? Because S-100 machines are not consumer-oriented, all-in-one microcomputers — but flexible, modular, professional-level systems that are easy to upgrade, modify, and adapt to specific applications. As a result, over the years the S-100 buss has proven to be the ideal choice for commercial, industrial, and scientific applications. It doesn't obsolete itself, but simply adapts to innovation.

We use the experience we've acquired in the past, coupled with the very best technology offered by the present, to build products for the future . . . products that meet, and often exceed, the demands of the new wave of professional S-100 users. Our expanded S-100 line is the right approach at the right time; we invite you to write for further information.

NEW! HIGH-PERFORMANCE S-100 MOTHERBOARDS

19 slot: $174 unkit*, $214 assm
12 slot: $129 unkit*, $169 assm
6 slot: $ 89 unkit*, $129 assm

*Edge connectors and termination resistors are pre-soldered in place for assembly.

These 3rd generation motherboards, designed to work with the latest 5 and 10 MHz CPUs coming on line, exceed the latest S-100 specs and offer superior performance. Includes true active termination (with half of the termination load at each end of every buss line), grounded Faraday shield between all buss signal lines to minimize crosstalk, and edge connectors included for all slots. All sizes fit Godbout, Vector, TEI, IMSAI, and similar enclosures.

These high quality motherboards are a welcome addition to any system — or the start of a great one.

2S "Interfacer" S-100 I/O board

$189 unkit, $249 assm, $324 CSC

Dual serial port with 2 full duplex parallel ports for RS-232 handshake; EIA232C line drivers and receivers (1488, 1489) along with current loop (20 mA) and TTL signals on both ports. On-board crystal controlled timebase with independently selectable Baud rate generators for each port (up to 19.2 KBaud). Hardware UARTs don't tie up the CPU. And, there's much more... this is a no-excuses serial board that does things the others only dream about.

NEW! 3P+S "Interfacer II" S-100 I/O board

$189 unkit, $249 assm, $324 CSC

Incorporates 1 channel of RS-232 serial I/O (with all the features of a port from the 2S "Interfacer", including handshaking), along with 3 full duplex parallel ports. The parallel section uses LSTTL octal latches for latched input and output data with 24 mA drive current, attention/enable/and strobe bits for each parallel port (with selectable polarity), interrupts for each input port, and separate 25 pin connectors with power for each channel along with a status port for interrupt mask and port status. All in all, this is an incredibly versatile and flexible board.

2708 S-100 EROM board

$85 unkit

4 independently addressable 4K blocks, with dipswitch selectable jump start built right into the board. Includes all support chips and manual, but does not included EROMs.

Active Terminator Board

$34.50 kit

Plugs into any S-100 motherboard (although ours don't need it) to reduce ringing, noise, crosstalk, and other buss-related problems. Here is an upgrade that is simple and effective.

The Godbout Box!

By the time you read this, we will be shipping our industrial-grade enclosure. It's perfectly suited to creating a powerful system based on our line of S-100 boards (or anyone else's, if you're so inclined). It's rack mount or desk mount (with sliders for pulling it out of the rack if desired), neat-looking, heavy duty, and comes with the back panel pre-punched to accept a variety of connectors. Oh yes, and let's not forget the power supply for powering all your boards; it comes with the box, too. **See your computer store for details, or write us direct.**

NEW! "MEMORY MANAGER" S-100 board

$59 kit, $85 assm, $100 CSC

Now you can add bank select and extended addressing to older S-100 machines like the Altair, IMSAI, Sol, Polymorphic, etc. Either use this board with our new extended addressing boards, or retrofit our high density **Econorams** (the ones with phantom or extra qualifier lines) for use with the **Memory Manager Board** to get up to ½ a megabyte of memory space for your computer.

We supply memory

All our **Econoram*** memory is fully static, zips along at 4 MHz with the Z-80 or 5 MHz with the 8085, supports a number of popular busses, is available from us through computer stores world-wide, includes a 1 year limited warranty, and comes in **three** configurations to suit your needs. For lowest cost, choose an **"unkit"** with sockets and bypass caps pre-soldered in place for an easy, one-evening assembly. When you just can't wait to get going, order our **assembled and tested** version. For critical systems, specify boards qualified under our **Certified System Component (CSC)** high-reliability program. These boards are extensively tested, burned in for 200 hours, and are immediately replaced in event of failure within 1 year of invoice date. Refer to chart below for pricing.

Name	Buss & Notes	Unkit	Assm	CSC
8K Econoram IIA	S-100	$149	$179	$239
16K Econoram IV	S-100	$269	$329	$429
16K Econoram VIIA-16	S-100	$279	$339	$439
24K Econoram VIIA-24	S-100	$398	$485	$605
16K Econoram IX	Dig Grp	$319	$379	n/a
32K Econoram IX	Dig Grp	$559	$639	n/a
32K Econoram X	S-100	$529	$649	$789
32K Econoram XI	SBC/BLC	n/a	n/a	$1050
16K Econoram XII	S-100 (1)	$329	$419	$519
24K Econoram XII	S-100 (1)	$429	$539	$649
32K Econoram XIII	S-100 (2)	$559	$699	$849
16K Econoram XIV	S-100 (3)	$289	$349	$448
16K Econoram XV-16	H8 (4)	$329	$395	n/a
32K Econoram XV-32	H8 (4)	$599	$729	n/a
16K Memory Expansion	(5)	$87.20	n/a	n/a

16K x 16 or 32K x 8 Econoram XVI — coming soon!

Notes
(1) Bank select board — 2 independent banks addressable on 8K boundaries.
(2) Bank select board — 2 independent banks addressable on 16K boundaries.
(3) Extended addressing (24 address lines). Single block addressable on 4K boundaries.
(4) Bank select option for implementing memory systems greater than 64K.
(5) Chip set expands memory in Radio Shack-80, Apple, and Exidy Sorcerer machines.

*Econoram is a trademark of Godbout Electronics.

KEYBOARD SPECIAL:

Microswitch keyboard, already encoded with upper and lower case ASCII. Silent switches (not reed type). Requires +5 and −12V. With edge connectors; just plug in and go. **Normally $99, but order merchandise worth $50 or more and the keyboard is yours for only $49!**

Season's Greetings and Happy New Year!

Thank you for the support that made 1979 a great year for us . . . we'll continue to earn that support in 1980.

TERMS: Cal res add tax. Allow 5% for shipping, excess refunded. VISA®/Mastercharge® call our 24 hour order desk at (415) 562-0636. COD OK with street address for UPS. Prices good through cover month of magazine.



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from



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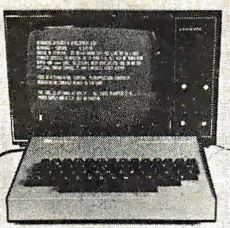
Circle 150 on inquiry card.

Listing 1 continued:

```
02ED C2E402          JNZ     C311      ;MORE TO GO
02F0 E1              POP     H         ;RESTORE X
02F1 2C              INR     L         ;UP ONE ON Y
02F2 C9              RET               ;END OF LOCAL SUBROUTINE
               ;
               ;BLOCK 4:  GENERATE FIRST COLUMN OF 5 WIDE CHARACTERS
               ;         A = 03H          C = CHAR - 32
               ;         D,E = XPOS, YPOS
               ;         H,L = ADDR OF 1ST BYTE OF CHAR TABLE ENTRY
               ;
02F3 7E        C400:  MOV     A,M       ;GET FLAGS
02F4 D5               PUSH    D         ;SAVE STARTING CURSOR
02F5 E604             ANI     04H       ;AUXILIARY LOOKUP REQUIRED
02F7 C21003           JNZ     C410      ;  YES.  GO DO IT
02FA 2F               CMA               ;1ST COLUMN ALL ONES (M & W)
02FB 0605      C411:  MVI     B,05H     ;5 POINTS TO A COLUMN
02FD 07        C401:  RLC               ;SHOULD THE POINT BE ON?
02FE EB               XCHG              ;GET X,Y IN H,L
02FF 22AC04           SHLD    YPOS      ;CURRENT CURSOR POSITION
0302 DC7701           CC      DOT       ;DISPLAY AS REQUIRED
0305 EB               XCHG              ;BACK TO NORMALCY
0306 1C               INR     E         ;NEXT YPOS
0307 05               DCR     B         ;TEST FOR DONE
0308 C2FD02           JNZ     C401      ;NOT YET
030B D1               POP     D         ;ORIGINAL CURSOR POSITION
030C 14               INR     D         ;FIX UP TO DO COLUMNS 2-5
030D 3E02             MVI     A,02H     ; AS A 4 WIDE CHAR
030F C9               RET
0310 E5        C410:  PUSH    H         ;SAVE CHAR TABLE ENTRY
0311 219A04           LXI     H,CHRA-3  ;AUXILIARY TABLE ADDR
0314 0600             MVI     B,00H     ;  FOR CHARS #, $, %, AND &
0316 09               DAD     B         ;NOTE: C HAS CHAR - 20H
0317 7E               MOV     A,M       ;GET THE FIRST COLUMN
0318 E1               POP     H         ;AND RESTORE TABLE ENTRY
0319 C3FB02           JMP     C411      ;DISPLAY THE RETRIEVED COLUMN
               ;
               ;BLOCK 5:  CONTROL CHARACTERS
               ;         A = ASCII CONTROL CHARACTER
               ;
031C FE00      C500:  CPI     00H       ;MAXR?
031E CA2603           JZ      C501      ;YES
0321 FE02             CPI     02H       ;R128?
0323 C23003           JNZ     C503      ;NO
0326 067F      C501:  MVI     B,7FH     ;128 BY 128 WHITE
0328 0F        C502:  RRC               ;CONVERT TO MODE BYTE
0329 32AF04           STA     MODE      ; AND SAVE NEW MODE
032C 78               MOV     A,B       ;GET DESIRED DAZZLER MODE
032D D30F             OUT     DAZ1      ;AND TELL THE DAZZLER
032F C9               RET
0330 FE01      C503:  CPI     01H       ;MAXC?
0332 CA3A03           JZ      C504      ;YES
0335 FE03             CPI     03H       ;R64?
0337 C23F03           JNZ     C505      ;NO
033A 063F      C504:  MVI     B,3FH     ;64 BY 64 FULL COLOR
033C C32803           JMP     C502      ;REST IS SAME AS 128
033F FE0A      C505:  CPI     0AH       ;LINE FEED?
0341 C24C03           JNZ     C506      ;NO
0344 21AC04           LXI     H,YPOS    ;YPOS = YPOS - 8
0347 7E               MOV     A,M
0348 D608             SUI     08H
034A 77               MOV     M,A
034B C9               RET
034C FE0D      C506:  CPI     0DH       ;CARRIAGE RETURN?
034E C25603           JNZ     C508      ;NO
0351 AF        C507:  XRA     A         ;XPOS = 0
0352 32AD04           STA     XPOS
0355 C9               RET
0356 FE0C      C508:  CPI     0CH       ;FORM FEED?
0358 C26D03           JNZ     C510      ;NO
035B 3AAF04           LDA     MODE      ;WHAT RESOLUTION?
035E 47               MOV     B,A
035F 3E7A             MVI     A,7AH     ;ASSUME 128 BY 128
0361 04               INR     B         ;IS IT?
0362 F26703           JP      C509      ;SURE IS
0365 3E3A             MVI     A,3AH     ;BAD ASSUMPTION
0367 32AC04    C509:  STA     YPOS      ;SO MUCH FOR YPOS
036A C35103           JMP     C507      ;TAKE CARE OF XPOS
036D FE10      C510:  CPI     10H       ;BLACK?
036F CA8303           JZ      C512      ;SURE IS
0372 D8               RC                ;NOT EVEN A COLOR
0373 FE18             CPI     18H       ;ABOVE WHITE?
0375 D0               RNC               ;YES.  FORGET IT
0376 F608             ORI     08H       ;USE BRIGHT COLORS
0378 47               MOV     B,A       ;SAVE WHERE SAFE
0379 3AAF04           LDA     MODE      ;128 BY 128 CAN ONLY
037C 3C               INR     A         ;  BE WHITE
037D FA8203           JM      C511      ;OK.  64 BY 64
0380 060F             MVI     B,0FH     ;FORCE IT TO BE WHITE
0382 78        C511:  MOV     A,B       ;MAKE BOTH HALFS
0383 E60F      C512:  ANI     0FH       ;  THE SAME
0385 47               MOV     B,A       ;SAVE ONE COPY
0386 0F               RRC
0387 0F               RRC
0388 0F               RRC
0389 0F               RRC
038A B0               ORA     B         ;COMPLETE COLOR BYTE
038B 32AE04           STA     COLOR
038E C9               RET

               ;
               ;ROUTINE ANIMAT
               ;         SWAP DISPLAY BUFFERS
               ;         BUFFER CURRENTLY BEING FILLED IS DISPLAYED
               ;         BUFFER INDICATED BY ANIM IS FILLED
               ;            ANIM=0    STARTS FILLING RBUF+2K
               ;            ANIM=-1   STARTS FILLING RBUF-2K
               ;
038F F5        ANIMAT: PUSH   PSW       ;SAVE REGISTERS USED
0390 C5                PUSH   B         ;
0391 E5                PUSH   H         ;D IS NOT TOUCHED
0392 DB0E      AN002:  IN     DAZ0      ;VERTICAL BLANKING ON?
0394 E640              ANI    40H       ;IF SO
0396 CA9203            JZ     AN002     ;  WAIT FOR NEXT ONE
0399 21AB04            LXI    H,ANIM    ;ADDRESS OF IN USE FLAG
039C 7E                MOV    A,M       ;  BUFFER IN USE
039D 2F                CMA              ;SET FOR NEXT TRY
039E 77                MOV    M,A       ;  AND SAVE FOR NEXT TIME
039F 47                MOV    B,A       ;  ALSO SAVE FOR LATER
```

Listing 1 continued on page 174



By Netronics

ASCII/BAUDOT, STAND ALONE

Computer Terminal

COMPLETE FOR ONLY . . . $149^95

The Netronics ASCII/BAUDOT Computer Terminal Kit is a microprocessor-controlled, stand alone keyboard/terminal requring no computer memory or software. It allows the use of either a 64 or 32 character by 16 line professional display format with selectable baud rate, RS232-C or 20 ma. output, full cursor control and 75 ohm composite video output.

The keyboard follows the standard typewriter configuration and generates the entire 128 character ASCII upper/lower case set with 96 printable characters. Features include onboard regulators, selectable parity, shift lock key, alpha lock jumper, a drive capability of one TTY load, and the ability to mate directly with almost any computer, including the new Explorer/85 and ELF products by Netronics.

The Computer Terminal requires no I/O mapping and includes 1k of memory, character generator, 2 key rollover, processor controlled cursor control, parallel ASCII/BAUDOT to serial conversion and serial to video processing—fully crystal controlled for superb accuracy. PC boards are the highest quality glass epoxy for the ultimate in reliability and long life.

VIDEO DISPLAY SPECIFICATIONS

The heart of the Netronics Computer Terminal is the microprocessor-controlled Netronics Video Display Board (VID) which allows the terminal to utilize either a parallel ASCII or BAUDOT signal source. The VID converts the parallel data to serial data which is then formatted to either RS232-C or 20 ma. current loop output, which can be connected to the serial I/O on your computer or other interface, i.e., Modem.

When connected to a computer, the computer must echo the character received. This data is received by the VID which processes the information, converting to data to video suitable to be displayed on a TV set (using an RF modulator) or on a video monitor. The VID generates the cursor, horizontal and vertical sync pulses and performs the housekeeping relative to which character and where it is to be displayed on the screen.

Video Output: *1.5 P/P into 75 ohm (EIA RS-170)* • **Baud Rate:** *110 and 300 ASCII* • **Outputs:** *RS232-C or 20 ma. current loop* • **ASCII Character Set:** *128 printable characters—*

αβγδεθιλμνπΣφ ωΩ 0123 02±÷≈∫|←→↑↓
!"#$%&'()*+,-./0123456789:;<=>?
@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_
`abcdefghijklmnopqrstuvwxyz{|}~

BAUDOT Character Set: *A B C D E F G H I J K L M N O P Q R S T U V W X Y Z - ? : * 3 $ # ( ) . , 9 0 1 4 ! 5 7 ; 2 / 6 8* • **Cursor Modes:** *Home, Backspace, Horizontal Tab, Line Feed, Vertical Tab, Carriage Return. Two special cursor sequences are provided for absolute and relative X-Y cursor addressing* • **Cursor Control:** *Erase, End of Line, Erase of Screen, Form Feed, Delete* • **Monitor Operation:** *50 or 60Hz (jumper selectable.*

Continental U.S.A. Credit Card Buyers Outside Connecticut

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Netronics R&D Ltd., Dept. PE-9
333 Litchfield Road, New Milford, CT 06776

Please send the items checked below—

- ☐ **Netronics Stand Alone ASCII Keyboard/Computer Terminal Kit, $149.95** plus $3.00 postage & handling.
- ☐ **Deluxe Steel Cabinet** for Netronics Keyboard/Terminal In Blue/Black Finish, **$19.95** plus $2.50 postage and handling.
- ☐ **Video Display Board Kit** alone (less keyboard), **$89.95** plus $3 postage & handling.
- ☐ **12" Video Monitor** (10 MHz bandwidth) fully assembled and tested, **$139.95** plus $5 postage and handling.
- ☐ **RF Modulator Kit** (to use your TV set for a monitor), **$8.95** postpaid.
- ☐ **5 amp Power Supply Kit** In Deluxe Steel Cabinet (±8VDC @ 5 amps, plus 6-8 VAC), **$39.95** plus $2 postage & handling.

Total Enclosed (Conn. res. add sales tax) $________
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Start Computing For Just $129.95 With An 8085-Based Professional Computer Kit—

Explorer/85

100% compatible with all 8080A and 8085 software & development tools!

No matter what your future computing plans may be, Level "A"—at $129.95—is your starting point.

Starting at just $129.95 for a Level "A" operating system, you can now build the exact computer you want. Explorer/85 can be your beginner's system, OEM controller, or IBM-formatted 8" disk small business system . . . yet you're never forced to spend a penny for a component or feature you don't want and you can expand in small, affordable steps!

Now, for just $129.95, you can own the first level of a fully expandable computer with professional capabilities—a computer which features the advanced Intel 8085 cpu, *thereby giving you immediate access to all software and development tools that exist for both the 8085 and its 8080A predecessor (they are 100% software compatible)*—a computer which features onboard S-100 bus expansion—plus instant conversion to mass storage disk memory with either 5-1/4" diskettes or standard IBM-formatted 8" disks.

For just $129.95 (plus the cost of a power supply, keyboard/terminal and RF modulator, if you don't have them already), Explorer/85 lets you begin *computing* on a significant level . . . *applying* the principles discussed in leading computer magazines . . . *developing* "state of the art" computer solutions for both the industrial and leisure environment.

Level "A" Specifications

Explorer/85's Level "A" system features the advanced Intel 8085 cpu, an 8355 ROM with 2k deluxe monitor/operating system, and an 8155 ROM-I/O—all on a single motherboard with room for RAM/ROM/PROM/EPROM and S-100 expansion, *plus* generous prototyping space.

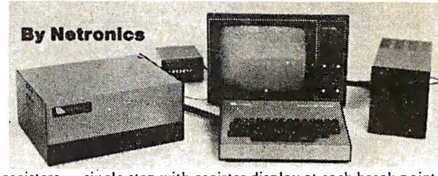
(Level "A" makes a perfect OEM controller for industrial applications and is available in a special Hex Version which can be programmed using the Netronics Hex Keypad/Display.)

Level "A" at $129.95 is a complete operating system, perfect for beginners, hobbiests, or industrial controller use.

PC Board: glass epoxy, plated through holes with solder mask • **I/O:** provisions for 25-pin (DB25) connector for terminal serial I/O, which can also support a paper tape reader . . . provision for 24-pin DIP socket for hex keyboard/display . . . cassette tape recorder input . . . cassette tape recorder output . . . cassette tape control output . . . speaker output . . . LED output indicator on SOD (serial output) line . . . printer interface (less drivers) . . . total of four 8-bit plus one 6-bit I/O ports • **Crystal Frequency:** 6.144 MHz • **Control Switches:** reset and user (RST 7.5) interrupt . . . additional provisions for RST 5.5, 6.5 and TRAP interrupts onboard • **Counter/Timer:** programmable, 14-bit binary • **System RAM:** 256 bytes located at F800, ideal for smaller systems and for use as an isolated stack area in expanded systems . . . RAM expandable to 64k via S-100 bus or 4K on motherboard.

System Monitor (Terminal Version): 2k bytes of deluxe system monitor ROM located at F000 leaving 0000 free for user RAM/ROM. Features include tape load with labeling . . . tape dump with labeling . . . examine/change contents of memory . . . insert data . . . warm start . . . examine and change all registers . . . single step with register display at each break point, a debugging/training feature . . . go to execution address . . . move blocks of memory from one location to another . . . fill blocks of memory with a constant . . . display blocks of memory . . . automatic baud rate selection . . . variable display line length control (1-255 characters/line) . . . channelized I/O monitor routine with 8-bit parallel output for high speed printer . . . serial console in and console out channel so that monitor can communicate with I/O ports.

System Monitor (Hex Version): Tape load with labeling . . . tape dump with labeling . . . examine/change contents of memory . . . insert data . . . warm start . . . examine and change all registers . . . single step with register display at each break point . . . go to execution address. Level "A" in the *Hex Version* makes a perfect controller for industrial applications and can be programmed using the Netronics Hex Keypad/Display.



By Netronics



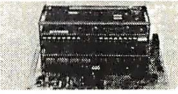
Hex Keypad/Display.

Hex Keypad/Display Specifications

Calculator type keypad with 24 system defined and 16 user defined keys. 6 digit calculator type display which displays full address plus data as well as register and status information.

Level "B" Specifications

Level "B" provides the S-100 signals plus buffers/drivers to support up to six S-100 bus boards and includes: address decoding for onboard 4k RAM expansion select-able in 4k blocks . . . address decoding for onboard 8k EPROM expansion selectable in 8k blocks . . . address and data bus drivers for onboard expansion . . . wait state generator (jumper selectable), to allow the use of slower memories . . . two separate 5 volt regulators.



Explorer/85 with Level "C" card cage.

Level "C" Specifications

Level "C" expands Explorer's motherboard with a card cage, allowing you to plug up to six S-100 cards directly into the motherboard. Both cage and cards are neatly contained inside Explorer's deluxe steel cabinet. Level "C" includes a sheet metal superstructure, a 5-card gold plated S-100 extension PC board which plugs into the motherboard. Just add required number of S-100 connectors

Level "D" Specifications

Level "D" provides 4k or RAM, power supply regulation, filtering decoupling components and sockets to expand your Explorer/85 memory to 4k (plus the original 256 bytes located in the 8155A). The static RAM can be located anywhere from 0000 to EFFF in 4k blocks.

Level "E" Specifications

Level "E" adds sockets for 8k of EPROM to use the popular Intel 2716 or the TI 2516. It includes all sockets, power supply regulator, heat sink, filtering and decoupling components. Sockets may also be used for soon to be available RAM IC's (allowing for up to 12k of onboard RAM).

Order A Coordinated Explorer/85 Applications Pak!

Experimenter's Pak (SAVE $12.50)—Buy Level "A" and Hex Keypad/Display for **$199.90** and get FREE Intel 8085 user's manual plus FREE postage & handling!

Student Pak (SAVE $24.45)—Buy Level "A," ASCII Keyboard/Computer Terminal, and Power Supply for **$319.85** and get FREE RF Modulator plus FREE Intel 8085 user's manual plus FREE postage & handling!

Engineering Pak (SAVE $41.00)—Buy Levels "A," "B," "C," "D," and "E" with Power Supply, ASCII Keyboard/Computer Terminal, and six S-100 Bus Connectors for **$514.75** and get 10 FREE computer grade cassette tapes plus FREE 8085 user's manual plus FREE postage & handling!

Business Pak (SAVE $89.95)—Buy Explorer/85 Levels "A," "B," and "C" (with cabinet), Power Supply, ASCII Keyboard/Computer Terminal (with cabinet), 16k RAM, 12" Video Monitor, North Star 5-1/4" Disk Drive (includes North Star BASIC) with power supply and cabinet, all for just **$1599.40** and get 10 FREE 5-1/4" minidiskettes ($49.95 value) plus FREE 8085 user's manual plus FREE postage & handling!

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333 Litchfield Road, New Milford, CT 06676

Please send the items checked below—

- ☐ **Explorer/85 Level "A" Kit** (ASCII Version), **$129.95** plus $3 p&h.
- ☐ **Explorer/85 Level "A" Kit** (Hex Version), **$129.95** plus $3 p&h.
- ☐ **8k Microsoft BASIC** on cassette tape, **$64.95** postpaid.
- ☐ **8k Microsoft BASIC in ROM Kit** (requires Levels "B," "D," and "E"), **$99.95** plus $2 p&h.
- ☐ **Level "B" (S-100) Kit, $49.95** plus $2 p&h.
- ☐ **Level "C" (S-100 6-card expander) Kit, $39.95** plus $2 p&h.
- ☐ **Level "D" (4k RAM) Kit, $69.95** plus $2 p&h.
- ☐ **Level "E" (EPROM/ROM) Kit, $5.95** plus 50¢ p&h.
- ☐ **Deluxe Steel Cabinet** for Explorer/85, **$49.95** plus $3 p&h.
- ☐ **ASCII Keyboard/Computer Terminal Kit** (features a full 128 character set, upper & lower case, full cursor control, 75 ohm video output convertible to baudot output, selectable baud rate, RS232-C or 20 ma. I/O, 32 or 64 character by 16 line formats, and can be used with either a CRT monitor or a TV set (if you have an RF modulator), **$149.95** plus $2.50 p&h.
- ☐ **Hex Keypad/Display Kit, $69.95** plus $2 p&h.
- ☐ **Deluxe Steel Cabinet** for ASCII Keyboard/Terminal, **$19.95** plus $2.50 p&h.
- ☐ **Power Supply Kit** (±8V @ 5 amps) in deluxe steel cabinet, **$39.95** plus $2 p&h.
- ☐ **Gold Plated S-100 Bus Connectors, $4.85** each, postpaid.
- ☐ **RF Modulator Kit** (allows you to use your TV set as a monitor), **$8.95** postpaid.
- ☐ **16k RAM Kit** (S-100 Board expands to 64k), **$199.95** plus $2 p&h.
- ☐ **32k RAM Kit, $329.95** plus $2 p&h.
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Listing 1 continued:

```
03A0 2B                  DCX     H          ;NOW LOOKING AT HIGH BYTE
03A1 7E                  MOV     A,M        ;  OF RBUF
03A2 37                  STC                ;FUTURE GO BIT
03A3 1F                  RAR                ;ALL SET TO DISPLAY
03A4 4F                  MOV     C,A        ;SAVE WHILE WAIT FOR VERT BLANK
03A5 DB0E        AN000:  IN      DAZ0       ;WHAT'S THE DAZZLER DOING?
03A7 E640                ANI     40H        ;VERTICAL BLANKING ON?
03A9 C2A503              JNZ     AN000      ;  NOT YET.  GIVE IT TIME
03AC 79                  MOV     A,C        ;NEW BUFFER WITH NO FLICKER
03AD D30E                OUT     DAZ0       ;  IS NOW DISPLAYING
03AF 7E                  MOV     A,M        ;CALCULATE NEW FILL
03B0 C608                ADI     08H        ;  ASSUME BUFFER 0
03B2 04                  INR     B          ;WHICH IS IT?
03B3 CAB803              JZ      AN001      ;ZERO IT IS
03B6 D610                SUI     10H        ;THE SECOND, SO COME BACK
03B8 77          AN001:  MOV     M,A        ;UPDATE THE FILL ADDRESS
03B9 E1                  POP     H          ;AND RESTORE THE WORLD
03BA C1                  POP     B          ;
03BB F1                  POP     PSW        ;
03BC C9                  RET                ;
                 ;
                 ;          END OF EXECUTABLE PROGRAM CODE
                 ;
                 ;          ********************************
                 ;
                 ;                   LOOKUP TABLES
                 ;
                 ;
                 ;MOVE TABLE FOR THE LINE GENERATOR
                 ;
03BD FF00FFFF    MXT:    DB      0FFH,000H,0FFH,0FFH        ;SECTOR 5
03C1 00FFFFFF            DB      000H,0FFH,0FFH,0FFH        ;SECTOR 6
03C5 FF00FF01            DB      0FFH,000H,0FFH,001H        ;SECTOR 4
03C9 0001FF01            DB      000H,001H,0FFH,001H        ;SECTOR 3
03CD 010001FF            DB      001H,000H,001H,0FFH        ;SECTOR 8
03D1 00FF01FF            DB      000H,0FFH,001H,0FFH        ;SECTOR 7
03D5 01000101            DB      001H,000H,001H,001H        ;SECTOR 1
03D9 00010101            DB      000H,001H,001H,001H        ;SECTOR 2
                 ;
                 ;
                 ;CHARACTER MATRIX TABLE
                 ;       EACH ENTRY IS 3 BYTES
                 ;       BIT >>  7    6    5    4    3    2    1    0
                 ;BYTE   0       U2   Q    R    S    T    V5   V2   V1
                 ;BYTE   1       M    N    O    P    I    J    K    L
                 ;BYTE   2       E    F    G    H    A    B    C    D
                 ;
                 ;       A  B  C  D                 FLAGS
                 ;       E  F  G  H        U2:  DESCENDERS, MOVE DOWN 2
                 ;       I  J  K  L        V2, V1:  WIDTH OF CHARACTER - 2
                 ;       M  N  O  P        V5:  FOR FIVE WIDE FIGURES
                 ;       Q  R  S  T                0 - FIRST COLUMN ALL ONES
                 ;                                 1 - FIRST COLUMN FROM CHRA
                 ;       REPRESENTS 2ND THRU 5TH COLUMNS
                 ;          OF FIVE COLUMN WIDE CHARACTERS
                 ;
                 CHRX:
D03DD 0200004008  DB  02H,00H,00H,40H,08H,88H,01H,00H,0AAH      ;   ! "
03E6 57FAFA775E   DB  57H,0FAH,0FAH,77H,5EH,4EH,1FH,0B4H,0A9H   ;# $ %
03EF 6F25CC0000   DB  6FH,25H,0CCH,00H,00H,88H,20H,88H,84H      ;& ' (
03F8 4044480 1A4  DB  40H,44H,48H,01H,0A4H,0A0H,01H,4EH,40H     ;) * +
0401 808800010E   DB  80H,88H,00H,01H,0EH,00H,40H,00H,00H       ;, - .
040A 42421032DB   DB  42H,42H,10H,32H,0DBH,96H,71H,44H,4CH      ;/ 0 1
0413 7A42967216   DB  7AH,42H,96H,72H,16H,1EH,0AH,1FH,99H       ;2 3 4
041C 721E8F329E   DB  72H,1EH,8FH,32H,9EH,86H,42H,42H,1FH       ;5 6 7
0425 3296967217   DB  32H,96H,96H,72H,17H,96H,40H,08H,00H       ;8 9 :
042E 8088081148   DB  80H,88H,08H,11H,48H,42H,01H,0E0H,0E0H     ;; < =
0437 4142482202   DB  41H,42H,48H,22H,02H,96H,62H,0BBH,9FH      ;> ? @
0440 4AF996729E   DB  4AH,0F9H,96H,72H,9EH,9EH,32H,98H,96H      ;A B C
0449 72999E7A8E   DB  72H,99H,9EH,7AH,8EH,8FH,42H,8EH,8FH       ;D E F
0452 329B864A9F   DB  32H,9BH,86H,4AH,9FH,99H,71H,44H,4EH       ;G H I
045B 3291114AAC   DB  32H,91H,11H,4AH,0ACH,0A9H,7AH,88H,88H     ;J K L
0464 0B55B14A9B   DB  0BH,55H,0B1H,4AH,9BH,0D9H,32H,99H,96H     ;M N O
046D 428E9E3AB9   DB  42H,8EH,9EH,3AH,0B9H,96H,4AH,0AEH,9EH     ;P Q R
0476 7216871222   DB  72H,16H,87H,12H,22H,2FH,32H,99H,99H       ;S T U
047F 3269990BB5   DB  32H,69H,99H,0BH,0B5H,51H,4AH,66H,99H      ;V W X
0488 2226997A84   DB  22H,26H,99H,7AH,84H,2FH,60H,88H,8CH       ;Y Z [
0491 0212486044   DB  02H,12H,48H,60H,44H,4CH,02H,00H,96H       ;/ ] ^
049A F80000       DB  0F8H,00H,00H                              ;_
                 ;AUXILIARY LOOKUP TABLE
                 ;       FIRST COLUMN OF #, $, %, AND &
                 ;
049D 50109860    CHRA:   DB      50H,10H,98H,60H ;# $ % &

                 ;
                 ;          END OF ROMABLE SEGMENT OF PROGRAM
                 ;
                 ;          ************************************
                 ;
                 ;          START OF RAM (VARIABLE) STORAGE AREA
                 ;
                 ;SCRATCH PAD STORAGE FOR THE LINE GENERATOR
                 ;       THESE LOCATIONS MAY BE ALTERED AT ANY TIME A
                 ;          LINE IS NOT ACTUALLY BEING GENERATED
                 ;       VARIABLES MUST BE IN THE ORDER GIVEN.
                 ;
04A1             DY:     DS      2       ;+YP
04A3             DX:     DS      2       ;- XP
04A5             M0X:    DS      1       ;X INCR FOR A ZERO MOVE
04A6             M0Y:    DS      1       ;Y INCR FOR A ZERO MOE
04A7             M1X:    DS      1       ;X INCR FOR A ONE MOVE
04A8             M1Y:    DS      1       ;Y INCR FOR A ONE MOVE
                 ;
                 ;
                 ;GLOBAL STORAGE AREA FOR THE GRAPHICS PACKAGE
                 ;       THESE LOCATIONS MUST BE PRESERVED BETWEEN
                 ;          CALLS TO THE GRAPHICS ROUTINES.
                 ;       THEY ARE INITIALIZED BY INITG.
                 ;       VARIABLES MUST BE IN THE ORDER GIVEN.
                 ;
04A9             RBUF:   DS      2       ;REFRESH BUFFER ADDRESS
04AB             ANIN:   DS      1       ;BUFFER IN USE FLAG FOR ANIMATIO
                                          N
04AC             YPOS:   DS      1       ;Y CURSOR VALUE
04AD             XPOS:   DS      1       ;X CURSOR VALUE
04AE             COLDB:  DS      1       ;CURRENT COLOR BYTE
04AF             MODE:   DS      1       ;DISPLAY MODE
04B0                     END
```

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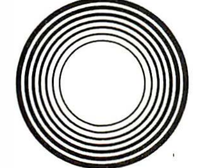
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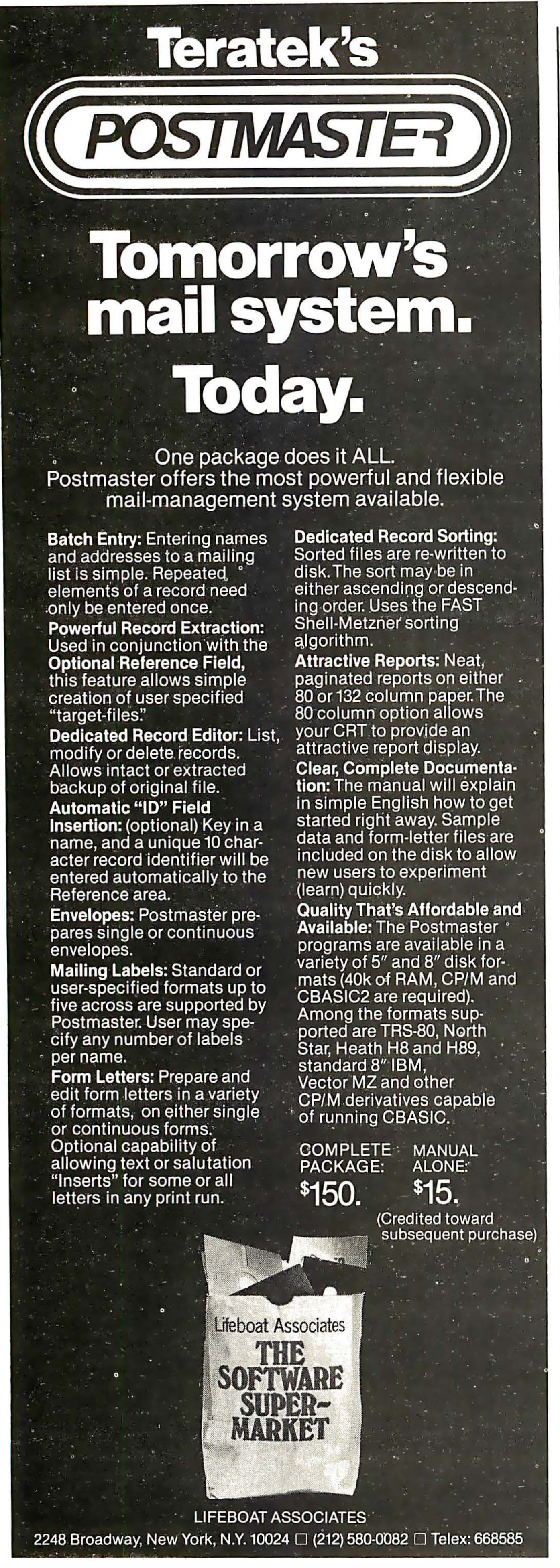
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Text continued from page 82:
cates that double buffered animation is available, MAXC mode has 15 colors and 64 by 64 resolution, the display is in color, and MAXR mode has one color and 128 by 128 resolution.

8080/Dazzler Page

The PAGE routine takes advantage of the hardware requirement that refresh buffers start only on even page boundaries and are 2 K bytes long. The low-byte of the address is used for a free zero, while the HL register is incremented until H corresponds to the high-byte of the first address beyond the buffer.

8080/Dazzler Cursor

Since the same scaling routine is used for both CURSOR and LINE, CURSOR becomes an almost empty routine. Aside from preserving registers, all it does is call CU000 with the coordinates presented, and save the scaled result as the new software cursor position XPOS, YPOS.

The MODE byte engages in some trickery to indicate the desired mode efficiently. The numeric value associated with the mode is rotated right one bit position. The resultant value can be incremented up to 126 times and still remain negative if in MAXC or R64 mode, and positive if in MAXR or R128 mode. Since MAXR on the Dazzler is 128 by 128 resolution, and MAXC is 64 by 64, we have a simple test to determine which mode is in use.

The scale routine CU000 divides X and Y by 2, checks to see if R128 or MAXR is selected, and divides again if they are not.

8080/Dazzler DOT

This routine tends to be somewhat complex due to the convoluted mapping from bits in the byte to points on the screen used by the Dazzler in 128 by 128 resolution mode, and the dividing of the screen into four quadrants. Fortunately, if the 128 by 128 coordinates are divided by 2, the address and mask generated by applying the algorithm for 64 by 64 resolution yields the four bits corresponding to the four possible 128 by 128 points. The low-order bits of the X and Y coordinates lost in the division are then used to select the single bit corresponding to the desired point.

The four quadrant problem is similarly solved by using the high-order bit of each coordinate to determine the quadrant, and the remaining lower order bits to find the location inside the quadrant. Since these problems are unique to the Dazzler, they will not be discussed further. The interested reader is invited to trace the logic in the program listing.

One final comment on the DOT routine is appropriate. The DOT register restore sequence is also used by LINE and CHAR. If it is changed, the appropriate modifications will also be required in LINE and CHAR.

8080/Dazzler LINE

The LINE routine is almost a block-for-block encoding of the LINE algorithm. The variable name correspondence table (table 8) is provided as a cross-reference guide, since some of the variable names used in the algorithm were modified.

Because the values of XP and YP are lost when the cursor adjustments for "move 0" and "move 1" are looked up, initialization of variables is moved to immediately after sector determination. TA and T0 are both 16-bit numbers because they represent the product of two 8-bit numbers. The only 16-bit arithmetic available on the 8080 is addition. To subtract X from T0, the 16-bit two's complement of X, DX, is calculated and added. Similarly, DY is the 16-bit representation of Y.

The cursor adjustments required for a "move 0" and a "move 1" are looked up in the table MXT. Entries are indexed by sector weight. Each entry is four bytes long (M0X, M0Y, M1X, and M1Y for the particular sector), so the sector weight is multiplied by 4 (two shifts left) and added to the starting address of the table. The correct cursor adjustments are then retrieved and stored where access is more convenient.

The only other significant change to the logic is the placement of the test for completion. For efficiency, x is compared to X immediately after the point is displayed. This has the added advantage of occurring at the only time the stack is free of temporary variables.

8080/Dazzler CHAR

The CHAR routine, with the exception of control character processing, also follows its Nassi-Schneiderman chart rigorously. The major change has been to convert to a SELECT construct the string of IFs used for control character processing. This avoids a multitude of tests which are guaranteed to fail once the character has been recognized. The processing of control characters with similar actions has also been consolidated to reduce redundancy.

As is obvious from its Nassi-Schneiderman chart, CHAR is really two independent routines with a common entry point. The only common code is the register saving and parity stripping. By pushing the address of the restore register routine onto the top of the stack, the return (RET) instruction will jump to the restore register sequence, restore all registers, and then return to the calling program.

The character matrix table is indexed by ASCII value minus 32, ie: the first entry is a blank. Since each entry is

Table 8: *Variable name definitions for LINE.*

8080 Software	Algorithm Description
XT	x
YT (not used)	y
XP	X
YP	Y
XPOS or XC	XC
YPOS or YC	YC
XF	XF
YF	YF
TA	TA
T0	T0
DX	−X
DY	+Y
M0X, M0Y	Cursor adjustment for a "Move 0"
M1X, M1Y	Cursor adjustment for a "Move 1"

Note: *The table numbering sequence is continued from part 1.*

three bytes long, the index must be multiplied by 3 to get the offset into the table. (The format of the character table is fully defined in the comments preceding it in the listing.) The first byte of each entry contains all the flags describing the character. The width bits are masked off and the cursor value for the next character position calculated. If the width is 6 (including a blank pixel between characters) the special subroutine to generate the first column of a 5-column wide character is executed. The descender indicator flag is then checked and the cursor is adjusted if necessary.

The normal character generation code scans the character matrix row-by-row. Whenever a 1 is encountered, the DOT routine is called to display the pixel at that location. When all five rows are completed, the cursor value is set for the next character position as calculated earlier, and control returned to the calling program.

The special subroutine used for five wide characters generates only the first column. By incrementing the cursor position, the normal character generation sequence is used to generate columns 2 through 5 instead of the normal 1 through 4.

Control character handling proceeds in three phases. Phase 1 checks for any of the four mode controls and sets MODE as required. The Dazzler hardware must also be informed so it can change mode. Phase 2 is entered if the control character is not a mode control. This is an individual check for each of the carriage control characters. Note that to get to the top line, form feed must determine what resolution is in use. Phase 3, if reached, is current color selection. The value of the control character is first checked to verify that it actually is a color select character. If it is black, the COLOR byte is set to all zeros. If any other color, a check is made to determine if the Dazzler is in a color supporting mode (MAXC or R64). If not, COLOR is set to all ones (high-resolution white). If a color mode is in use, the bright bit is set and the low-order four bits are duplicated in the high-half of the byte to yield a COLOR byte with the desired color in both pixel fields. Conveniently, the Dazzler color bit definitions match the lower three bits of the color select character.

A word of caution is in order for anyone using the compiler hexadecimal output in the listing directly, rather than the source code. The character table contains more bytes per line than the compiler used allocates for listing purposes (hence the "D" error). One must load the character table from the source code rather than from the compiler's hexadecimal output.

8080/Dazzler ANIMAT

The ANIMAT routine's implementation is adequately described in the comments on the listing. The flag byte ANIM indicates whether the first 2 K buffer or the second (auxiliary) 2 K buffer is currently being filled. Note that if the buffer swap were made as soon as vertical blanking was detected rather than as soon as vertical blanking was detected following an absence of vertical blanking, it would be possible to swap buffers, modify the display, and swap buffers again—all during one vertical blanking period. The net result, of course, would be that the one buffer would never be displayed, a clearly undesirable circumstance.

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Circle 233 on inquiry card.

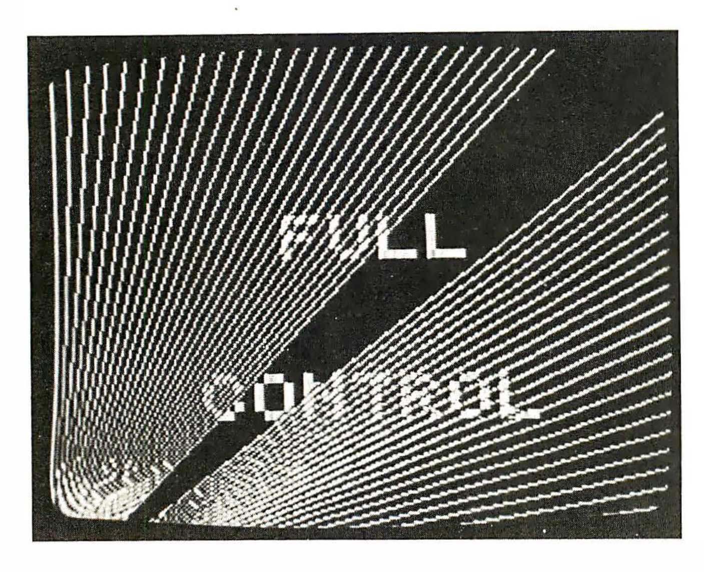


Photo 1: *Display generated by demonstration program number 2 (see listing 2).*

Photo 2: *Display generated by demonstration program number 3 (see listing 2).*

Demonstration Program

The demonstration program (see listing 2 on page 184) is provided for several purposes. Aside from demonstrating the power of the protocols, it serves as a tutorial in using the 8080 assembly language protocol and as a debugged, working user program for verifying successful implementation of the 8080 assembly language protocol. The photographs illustrating this article were all generated by this program and a Matrox ALT-256**2 display. The program contains four independent demonstrations and two utility subroutines. Equates are used to allow mnemonic references to the standard protocol's entry vectors, color controls, and display modes.

The first demonstration is a maximum-resolution exercise for the line generator. The identification message uses R64 resolution deliberately to get large characters. A series of maximum-length lines are drawn to generate the string art parabolas in each corner. The calculation of the endpoints of all the lines is simplified by the standard coordinate system. Their spacing is controlled by the value for MRSCLF returned by INITG. Because of the speed of generation, a variable delay utility subroutine, PAUSE, is used to give time to observe the display. These pauses may be extended indefinitely by setting the switch register to hexadecimal 01.

The second demonstration tests the generation of all 64 of the uppercase ASCII characters. Again, advantage is taken of the lowest resolution mode to display large characters. The 64 characters are drawn eight times, once in each color, in order to demonstrate the ability to vary the display dynamically. On the last iteration, the characters are drawn in black, leaving a clear screen. Rather than verify that the display is capable of selective erase, the PAGE routine is also called. The full range of available character sizes is then displayed using R64, MAXR, and R128 display modes for one line each. All mode changes are immediately followed by absolute cursor positioning commands to avoid erroneous results.

The third demonstration cycles through all available colors with the line generator. To avoid claiming Full Color Control on a monochrome display, the color bit in MAXCD is tested. MCCOLS is then checked to see how many colors or grey shades are available. All available colors are used, one at a time, as one end of each line is moved closer to (255,255). The attempt at mode RXXX, after shifting to R64, is ignored by the package in this article. The enhanced Dazzler package available from Cromemco uses it to select the Dazzler's 16-level grey scale mode.

The final demonstration is a short animation sequence. The header is inserted in both buffers. The auxiliary buffer must be cleared first, since this function is not included in the standard. If the display is not double buffered, this will also clear any warning messages generated by the graphics package.

The algorithm used to animate the figure will work with either double buffered displays or selectively erasable displays. For the former, the figure is backed up one step and drawn in black to erase it from the nondisplaying buffer (PAGE would require too much time and erase the header). The figure is then advanced two steps to get to the position past the one currently being displayed and drawn in white. Finally, ANIMAT is called to display the updated buffer, and the whole procedure is repeated until the screen is traversed. If the display is not double buffered (tested using the ANIM field in MAXRD), the ANIMAT routine is called anyway to delay until the start of vertical blanking. While the display is busy with vertical blanking, the old figure is erased and the new one displayed. If all the changes can be made before the affected memory is displayed, there will not be any flicker, and the animation will be as smooth as when double buffering is used.

The STRING subroutine is a convenient utility for displaying text strings. It calls the CHAR routine with each successive character in a string of ASCII characters until an ASCII '$' (hexadecimal 24) is detected.

Conclusion

The availability of a powerful graphics protocol immensely simplifies the design and coding of graphics programs. The limitations imposed by forcing individual capabilities to meet a common protocol are more than made up by the availability of precisely defined functions and controls. Furthermore, the protocol is sufficiently flexible to allow the installation and use of unique display features without adversely affecting the ability to run programs designed to the standard. For example, the package available from Matrox for its ALT-256**2 contains such enhancements as high-resolution positioning of low-resolution DOTs, choice of fixed or proportional character spacing, and up to 8 bits (256 combinations) color and/or grey scale for each pixel.

The author would like to thank John Rogers, Gary Johnsey, and especially Bart Schwartz for their help in making these articles possible.

Graphics Interface Standard for FORTRAN

The following FORTRAN subroutine definitions extend the flexibility and hardware independence of the proposed microcomputer graphics standard to FORTRAN.

INITG (XMRSCL, YMRSCL, MRCOLS, XMCSCL, YMCSCL, MCCOLS, LANIM, LCOLOR)

Initialize graphics hardware and software to maximum resolution mode with all options disabled. The screen is cleared and the current color is set to white. Eight variables are used to return the display parameters:

*XMRSCL (REAL*4) X dimension of physical display points in standard coordinates, maximum resolution mode.*
*YMRSCL (REAL*4) — as above except Y dimension.*
*MRCOLS (INTEGER*2) — colors (grey shades) available in maximum resolution mode.*
*XMCSCL (REAL*4) — X dimension of physical display points maximum colors mode.*
*YMCSCL (REAL*4) — as above except Y dimension.*
*MCCOLS (INTEGER*2) — colors (grey shades) available in maximum color selection mode.*
*LANIM (LOGICAL*1) — TRUE if double buffered animation available.*
*LCOLOR (LOGICAL*1) — TRUE if display is in color, FALSE implies monochrome.*

PAGE

Clear the sreen

CURSOR (IX, IY)

Move the cursor to the coordinate position specified.

*IX (INTEGER*2) — X (horizontal) coordinate desired. Value is in standard display coordinates (0 through 255). Out of range values are permitted but may have unpredictable results.*

*IY (INTEGER*2) — as above except Y (vertical) coordinate desired. Lower left-hand corner of the screen is the point 0,0.*

DOT

Display a dot at the current cursor position using the current color.

LINE (IX, IY)

Display a line from the current cursor position to the coordinate position specified. IX and IY are defined as in CURSOR.

CHAR (ICHAR)

The ASCII character defined by the low-order 7 bits of ICHAR is displayed at the current cursor position. Control characters are interpreted as defined in the standard to change display mode, current color, etc.

*ICHAR (INTEGER*2) — the ASCII character to be interpreted or displayed.*

ANIM

Program execution is delayed until the start of the next vertical blanking period. If double buffered animation is supported, buffers are not switched until immediately before returning.

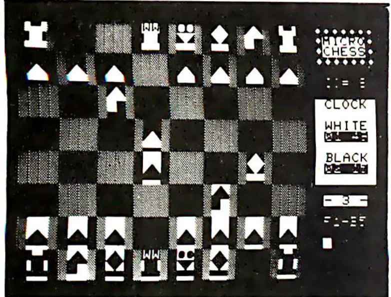
WRITE (10, nnn) var, var, ...

The logical unit number 10 is available for formatted output to the display. Binary output will result in an I/O (input/output) error. Input attempts will return End of File. Rewind, endfile, and backspace operations are no-ops. The display must be initialized by INITG before writing to LUN 10. The first character output on each line is interpreted as a standard FORTRAN printer control character (' ' for single space, '0' for double space, '1' for new page, and '+' to overprint the same line).

Sample Program

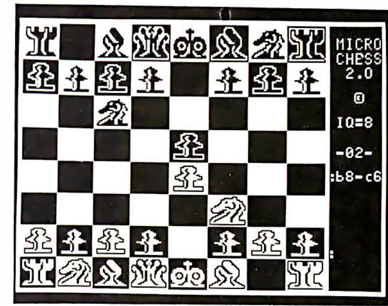
```
C---  Example usage of FORTRAN Standard Graphics Calls
      LOGICAL*1 LANIM, LCOLOR
C---  Initialize graphics
      CALL INITG(XMRSCL, YMRSCL, MRCOLS, XMCSCL,
     1 YMCSCL, MCCOLS, LANIM, LCOLOR)
C---  Title display
      WRITE (10, 100)
100   FORMAT(1H1, 'A SINE WAVE')
C---  Calculate and display a sine wave
C---  Move to starting point
      CALL CURSOR (0, 128)
C---  Determine distance between X values
      INCR = IFIX (YMRSCL + 0.5)
      IF(INCR.LE.0)INCR = 1
C---  Draw the actual curve
      DO 1000 IX = INCR, 255, INCR
      X = 3.14159*FLOAT(IX)/64.0
      Y = SIN(X)*100.0
      IY = IFIX (Y + 128.0)
1000  CALL LINE (IX, IY)
      END
```

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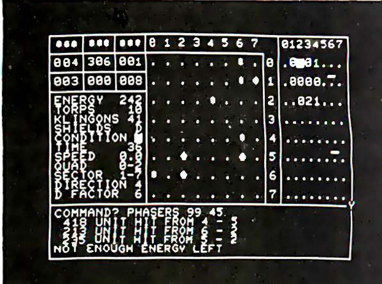


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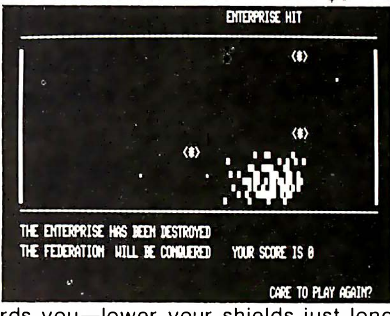


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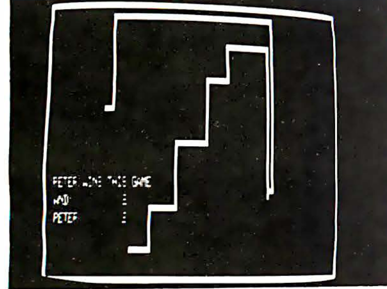


TIME TREK

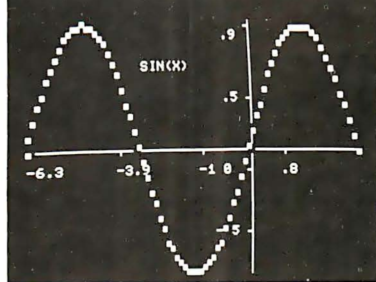
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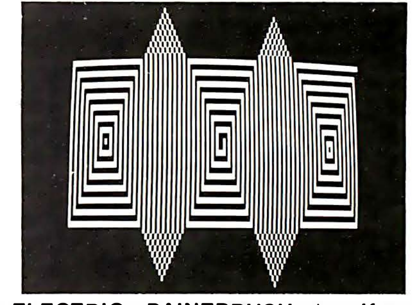
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Listing 2: *Four demonstration programs and two utility subroutines associated with the 8080 assembly language protocol for the proposed software standard. The first demonstration is a maximum-resolution exercise for the line generator. The second is a test of all 64 ASCII characters, which are drawn eight times, once in each color, in order to demonstrate the ability to dynamically vary the display. The third demonstration cycles through all available colors with the line generator. The final demonstration is a short animation sequence. STRING is used to display text strings.*

```
                ;       GRAPHICS PACKAGE DEMONSTRATION PROGRAM
                ;           VERSION 2.05B  <>  JULY 28,1977
                ;
                ;       ********* COPYRIGHT NOTICE *********
                ;       *                                  *
                ;       *                                  *
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                ;       *                                  *
                ;       ************************************
                ;
0500                    ORG     500H    ;START AFTER GRAPHICS PACKAGE
                ;;
                ;DEFININTION OF GRAPHICS PACKAGE ENTRY POINTS
                ;
0104 =                  INITG   EQU     104H
0107 =                  PAGE    EQU     107H
010A =                  CURSOR  EQU     10AH
010D =                  DOT     EQU     10DH
0110 =                  LINE    EQU     110H
0113 =                  CHAR    EQU     113H
0116 =                  ANIMAT  EQU     116H

                ;
                ;   AND STANDARD COLORS
                ;
0010 =                  BLK     EQU     10H     ;DELETE
0011 =                  RED     EQU     11H     ;RED
0015 =                  YEL     EQU     15H     ;YELLOW
0014 =                  GRN     EQU     14H     ;GREEN
0016 =                  CYN     EQU     16H     ;CYAN
0012 =                  BLU     EQU     12H     ;BLUE
0013 =                  MAG     EQU     13H     ;MAGENTA
0017 =                  WHI     EQU     17H     ;WHITE

                ;
                ;   AND TIMES FOR PAUSE (ASSUMES 2MHZ CLOCK)
                ;
0001 =                  HALF    EQU     1               ;HALF A SEC
0002 =                  ONE     EQU     2
0004 =                  TWO     EQU     4
000A =                  FIVE    EQU     0AH
0014 =                  TEN     EQU     14H

                ;
                ;   AND DISPLAY MODES
                ;
0000 =                  MAXR    EQU     00H             ;MAXIMUM RESOLUTION
0001 =                  MAXC    EQU     01H             ;MAXIMUM COLOR CHOICE
0002 =                  R128    EQU     02H             ;128 BY 128
0003 =                  R64     EQU     03H             ;64 BY 64
0004 =                  RXXX    EQU     04H             ;WHO KNOWS... BUT IT MAY
                ;
                ;       HERE STARTS THE ACTUAL PROGRAM
                ;
0500 312D09     DEMO:   LXI     SP,STACK        ;INIT STACK
0503 212E09             LXI     H,STACK+1       ;1ST FREE LOC
0506 CD0401             CALL    INITG   ;GET THE DISPLAY GOING
0509 222B08             SHLD    MAXCD   ;SAVE DISPLAY PARAMETERS
                ;
                ;DEMO #1:   HIGH RESOLUTION LINE DEMO
                ;
050C 3E03       DEM1:   MVI     A,R64   ;64 BY 64 MODE
050E CD1301             CALL    CHAR
0511 21A45C             LXI     H,5CA4H ;PUT UP LOGO
0514 CD0A01             CALL    CURSOR
0517 21BB07             LXI     H,STR30 ;BYTE
051A CD9107             CALL    STRING
051D 218034             LXI     H,3480H
0520 CD0A01             CALL    CURSOR
0523 21C707             LXI     H,STR01 ;GRAPHICS
0526 CD9107             CALL    STRING
0529 215C34             LXI     H,345CH
052C CD0A01             CALL    CURSOR
052F 21D207             LXI     H,STR02 ;STANDARD
0532 CD9107             CALL    STRING
0535 060A               MVI     B,FIVE  ;LET PEOPLE READ IT
0537 CDA107             CALL    PAUSE
053A 3E00               MVI     A,MAXR  ;SHIFT TO MAX RES
053C CD1301             CALL    CHAR
053F 01FF00             LXI     B,00FFH ;EXTREMES OF DISPLAY
0542 58                 MOV     D,B     ;D = CURRENT STEP
0543 79         DEM01:  MOV     A,C     ;E = MAX - CURRENT
0544 92                 SUB     D
0545 5F                 MOV     E,A
0546 62                 MOV     H,D     ;STARTING POINT
0547 68                 MOV     L,B     ; IS D,0
0548 CD0A01             CALL    CURSOR
054B 61                 MOV     H,C     ;TO 255,D
054C 6A                 MOV     L,D
054D CD1001             CALL    LINE
0550 63                 MOV     H,E     ;TO 255-D,255
```

Listing 2 continued on page 188

December 1, 1979



To the users of OMSI Pascal-1 for the PDP-11:

We are pleased to make available to you the new version (V1.2) of OMSI Pascal-1. V1.2 contains many enhancements and improvements, and you will find it easier to operate and even more reliable. The following overview outlines the most significant changes incorporated in the new version. For details, please ask for the V1.2 Language Specification and User's Guide(s).

Extended precision real arithmetic: a compiler switch causes all real calculations to be carried out with 15 digit precision (standard PDP-11 double precision four-word format). Extended precision is supported on all PDP-11 and LSI-11 processors, and on all operating systems. The precision of the library functions is also extended.

Debugger: the interactive debugger is now entirely Pascal-oriented, and is conversant with all user identifiers, types, scope rules, and the source program. The debugger has the capability, for example, to intercept a fatal error and display the last executed statements, or to accept and store commands for display of variables at a breakpoint.

Profiler: if you have ever wondered where your program spends its time, the Profiler can produce a listing and show you the number of times every line is executed.

Fatal error recovery: the system error procedure can be replaced by a Pascal-coded routine.

Direct access files: the procedure Seek(file,record) is a built-in procedure, and causes the file buffer to be positioned to any desired record.

File options: many enhancements have been made in file processing, allowing (for example) large buffers and spanned records on RSTS and RT11, and RSX file attributes including variable-length records. The RSTS file support uses 24-bit block numbers for RSTS V7 large file capability. All systems now support a full default filename when opening files.

Fast MACRO: most of the compilation time is actually spent in MACRO and the linking loader. On RSTS systems, a new utility (MAC) performs both of these functions in one-third of the time.

String package: included with V1.2 is a set of procedures and functions for handling dynamic length character strings. The package is written for portability in Standard Pascal.

Order information: to OMSI Pascal-1 licensees in warranty or extended support, V1.2 is available for the cost of handling, media, and shipping; other parties please contact Anne Smith, Vice-president for Sales.

Yours truly,

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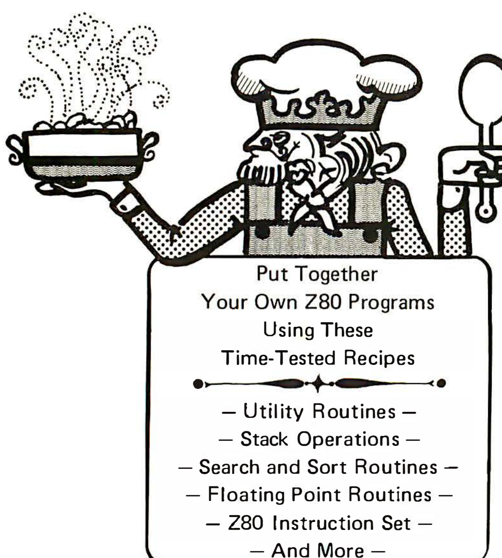
- *Straight lines*
- *Triangles*
- *Circles*
- *Elipses*
- *Borders*
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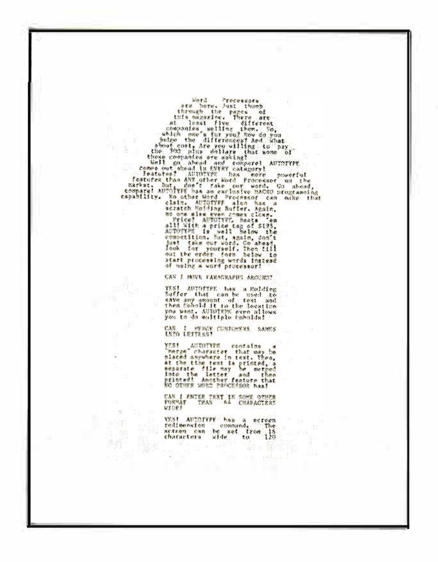
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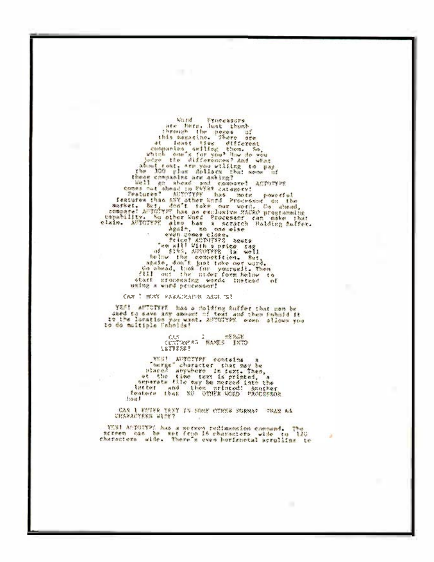
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Listing 2 continued:

```
0551 69                  MOV    L,C
0552 CD1001              CALL   LINE
0555 60                  MOV    H,B     ;TO 0, 255-D
0556 6B                  MOV    L,E
0557 CD1001              CALL   LINE
055A 62                  MDV    H,D     ;AND FINALLY...
055B 68                  MOV    L,B     ;  BACK TO D,0
055C CD1001              CALL   LINE
055F 3A2C08              LDA    MAXRD   ;DETERMINE NEXT D
0562 E607                ANI    07H     ;WIDTH OF A POINT
0564 C26805              JNZ    DEM12   ;MAKE SURE AT LEAST ONE
0567 3C                  INR    A
0568 17         DEM12:   RAL            ;MOVE 8 DISPLAY POINTS
0569 17                  RAL
056A 17                  RAL
056B 82                  ADD    D       ;D = D + RES*8
056C 57                  MOV    D,A
056D D24305              JNC    DEM01   ;D .LE. 255... MORE TO GO
0570 0614                MVI    B,TEN
0572 CDA107              CALL   PAUSE   ;SHOW IT OFF A BIT
                ;
                ;DEMO #2:   SHOW OFF CHARACTER SET
                ;
0575 CD0701              CALL   PAGE
0578 3E03                MVI    A,R64   ;USE BIGGEST CHARACTERS POSSIBLE
057A CD1301              CALL   CHAR
057D 0E07                MVI    C,7     ;INIT COLOR COUNTER
057F 3E10       DEM2:    MVI    A,BLK   ;START OUT WHITE
0581 81                  ADD    C
0582 CD1301              CALL   CHAR
0585 0620                MVI    B,' '   ;1ST CHAR IS BLANK
0587 21D808              LXI    H,08D8H ;UPPER LEFT CORNER
058A CD0A01     DEM20:   CALL   CURSOR  ;POSITION CHARACTER
058D 78                  MOV    A,B     ;WHAT CHAR THIS TIME
058E CD1301              CALL   CHAR
0591 3E20                MVI    A,20H   ;MOVE OVER TO NEXT POSITION
0593 84                  ADD    H
0594 67                  MOV    H,A
0595 D29F05              JNC    DEM21   ;PAST END OF LINE?
0598 7D                  MOV    A,L     ;MOVE DOWN TO NEXT
0599 D620                SUI    20H
059B 6F                  MOV    L,A
059C DAA305              JC     DEM22   ;DONE IF OFF BOTTOM
059F 04         DEM21:   INR    B       ;NEXT CHARACTER
05A0 C38A05              JMP    DEM20
05A3 0602       DEM22:   MVI    B,ONE   ;LOOK AT IT A BIT
05A5 CDA107              CALL   PAUSE   ;AREN'T THEY PRETTY?
05A8 0D                  DCR    C       ;TRY A NEW COLOR
05A9 F27F05              JP     DEM2    ;GO UNTIL ERASE
05AC CD0701              CALL   PAGE    ;JUST IN CASE A TEK 4010
05AF 21C04D              LXI    H,4DC0H ;MUST BE IN R64 AT THIS POINT
05B2 CD0A01              CALL   CURSOR
05B5 210208              LXI    H,STR06 ;'LARGE' + SHIFT TO MAXR
05B8 CD9107              CALL   STRING
05BB 218069              LXI    H,6980H
05BE CD0A01              CALL   CURSOR
05C1 210A08              LXI    H,STR07 ;'AND SMALL' + SHIFT TO R128
05C4 CD9107              CALL   STRING
05C7 21404D              LXI    H,4D40H
05CA CD0A01              CALL   CURSOR
05CD 211508              LXI    H,STR08 ;'CHARACTERS'
05D0 CD9107              CALL   STRING
05D3 0614                MVI    B,TEN   ;LET THAT SOAK IN
05D5 CDA107              CALL   PAUSE   ;  FOR A WHILE
05D8 CD0701              CALL   PAGE    ;CLEAR FOR NEXT DEMO
                ;
                ;DEMO #3:   FULL COLOR CONTROL
                ;
05DB 3E03                MVI    A,R64   ;LARGE LABELS
05DD CD1301              CALL   CHAR
05E0 21985C              LXI    H,5C98H
05E3 CD0A01              CALL   CURSOR
05E6 21DD07              LXI    H,STR03 ;'FULL' + COLOR SELECT
05E9 CD9107              CALL   STRING
05EC 3A2B08              LDA    MAXCD   ;COLOR CHOICE AVAILABLE?
05EF E670                ANI    70H     ;2 OR MORE?
05F1 0E11                MVI    C,BLK+1 ;ASSUME NOT
05F3 CA1906              JZ     DEM3X   ;GOOD ASSUMPTION
05F6 0E17                MVI    C,WHI   ;ASSUME 8 COLOR
05F8 E640                ANI    40H     ;MORE THAN 8?
05FA CAFF05              JZ     DEM3X1  ;  NOPE... GOOD ASSUMPTION
05FD 0E1F                MVI    C,BLK+15 ;GO FOR 16 COLORS
05FF 217450     DEM3X1:  LXI    H,5074H
0602 CD0A01              CALL   CURSOR
0605 3A2B08              LDA    MAXCD   ;COLOR OR MONOCHROME?
0608 E680                ANI    80H     ;  CHECK THE BIT
060A C21306              JNZ    DEM3X2  ;COLOR IT IS
060D 21EE07              LXI    H,STR04G ;'TONAL'
0610 C31606              JMP    DEM3X3
0613 21E307     DEM3X2:  LXI    H,STR04 ;'COLOR' IN COLOR
0616 CD9107     DEM3X3:  CALL   STRING
0619 21503C     DEM3X:   LXI    H,3C50H
061C CD0A01              CALL   CURSOR
061F 21F907              LXI    H,STR05 ;'CONTROL' IN WHITE
0622 CD9107              CALL   STRING
0625 1600                MVI    D,00H   ;INIT COUNTER
0627 3E01                MVI    A,MAXC  ;MAXIMUM COLORS (GREY SHADES)
0629 CD1301              CALL   CHAR
062C 59         DEM30:   MOV    E,C     ;START OUT WHITE
062D 26FF       DEM3:    MVI    H,0FFH  ;FROM TOP RIGHT SIDE
062F 7A                  MOV    A,D     ;WHICH STEP
0630 E63F                ANI    3FH     ;NORMALIZE TO 64
0632 17                  RAL            ;AND SCALE BACK
0633 17                  RAL            ;  TO 256
0634 6F                  MOV    L,A
0635 CD0A01              CALL   CURSOR
0638 210000              LXI    H,0000H ;TO LOWER LEFT CORNER
063B CD1001              CALL   LINE
063E 2EFF                MVI    L,0FFH  ;UP TO TOP EDGE
0640 67                  MOV    H,A
0641 CD1001              CALL   LINE
0644 14                  INR    D       ;NEXT STEP
```

Listing 2 continued on page 192





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Price? AUTOTYPE beats 'em all! With a price tag of $195, AUTOTYPE is well below the competition. But, again, don't just take our word. Go ahead, look for yourself. Then fill out the order form below to start processing words instead of using a word processor!

CAN I MOVE PARAGRAPHS AROUND?

YES! AUTOTYPE has a Holding Buffer that can be used to save any amount of text and then Unhold it to the location you want. AUTOTYPE even allows you to do multiple Unholds!

CAN I MERGE CUSTOMERS NAMES INTO LETTERS?

YES! AUTOTYPE contains a "merge" character that may be placed anywhere in text. Then, at the time text is printed, a separate file may be merged into the letter and then printed! Another feature that NO OTHER WORD PROCESSOR has!

CAN I ENTER TEXT IN SOME OTHER FORMAT THAN 64 CHARACTERS WIDE?

YES! AUTOTYPE has a screen redimension command. The screen can be set from 16 characters wide to 120 characters wide. There's even horizontal scrolling to view the text! Once more, we're far beyond the competition!

CAN IT HANDLE TEXT LARGER THAN MY COMPUTERS MEMORY?

YES! Most other Word Processors demand that the entire text be inside the computer. AUTOTYPE allows you to "spool" your text from the disk. This means that you can have edit files that are over 200 type written pages long!!

CAN IT UNDERLINE?
CAN IT BOLDFACE?
CAN IT INDENT?
CAN IT HYPHENATE?

YES! YES! YES! YES! AUTOTYPE has ALL the standard Word Processor features including underlining text, boldface printing and paragraph indentation. AUTOTYPE also has soft and hard hyphens. Soft hyphens are used at the end of lines and disappear if moved!

WHAT ABOUT INSERTING IN THE MIDDLE OF A WORD?

Certainly! AUTOTYPE allows inserting anything anywhere! You can move single letters or entire chapters right into the middle of any word. Now THAT'S POWER!

CAN IT SEARCH AND REPLACE?

YES! But, there's more! AUTOTYPE allows simple searches or search and replace. AUTOTYPE also allows wild card characters in the search string for probable matching! A very simple feature that AUTOTYPE makes very powerful!

CAN IT DO AUTOMATIC PAGE NUMBERING AND TITLING?

Of Course! Any length title up to the current line length. Page numbers can start anywhere. And if that's not enough, the number of blank lines below the title is adjustable!

DOES IT HAVE "DYNAMIC" PRINT FORMATTING?

OH YES! And with a flare! The pages that you see printed here were all printed from the same file. Only the print MACRO was altered! What's more, they were all printed on a standard serial printer. Complete "dynamic" print formatting can be accomplished with NO alteration of text!! Let's see the competition make that claim!

CAN IT DO SUBSCRIPTS AND SUPERSCRIPTS?

YES! Once again, AUTOTYPE has the features to be called a true processor of words and not just another word processor.

CAN IT VERTICAL TAB?

YES! And do negative vertical tabs to the top of page also! This is invaluable for two column printing.

CAN YOU ADJUST THE INDENT, LINE LENGTH AND JUSTIFICATION?

COMPLETELY! Either in the text itself, by manual formatting commands or with a print MACRO. Only AUTOTYPE gives you that kind of choice!

WILL IT EXECUTE A SERIES OF COMMANDS AUTOMATICALLY?

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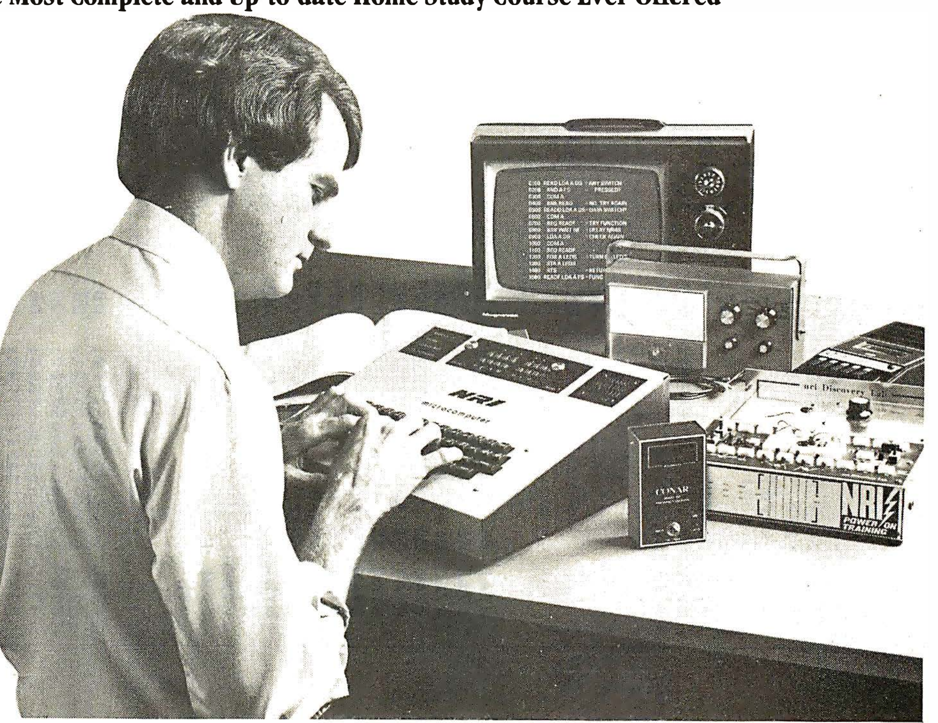
Listing 2 continued:

```
0645 CA9706          JZ    DEM4     ;256 STEPS AND ALL DONE
0648 7A              MOV   A,D      ;WHAT ARE WE ON?
0649 FE40            CPI   40H
064B DA6406          JC    DEM31    ;FULL COLOR, SLOW
064E CA7806          JZ    DEM32    ;SHIFT TO R64
0651 FE80            CPI   80H
0653 DA6406          JC    DEM31    ;R64, SLOW
0656 CA8D06          JZ    DEM33    ;BACK TO FULL COLOR
0659 FEC0            CPI   0C0H
065B DA6906          JC    DEM34    ;FULL COLOR, FULL SPEED
065E CA9206          JZ    DEM35    ;SHIFT TO ERASE
0661 C32D06          JMP   DEM3     ;FULL SPEED ERASE
0664 0601    DEM31:  MVI   B,HALF   ;SLIGHT PAUSE
0666 CDA107          CALL  PAUSE
0669 1D      DEM34:  DCR   E
066A 7B              MOV   A,E      ;DONE BLACK YET?
066B FE10            CPI   BLK
066D F27106          JP    DEM37    ;NOPE
0670 59              MOV   E,C      ;START OVER
0671 7B      DEM37:  MOV   A,E      ;NEW COLOR
0672 CD1301  DEM38:  CALL  CHAR     ;  (OR MAYBE MODE)
0675 C32D06          JMP   DEM3
0678 3E03    DEM32:  MVI   A,R64    ;SHIFT TO 64 BY 64
067A CD1301          CALL  CHAR
067D 3E04            MVI   A,RXXX   ;TRY FOR SOMETHING SPECIAL!
067F 0604    DEM36:  MVI   B,TWO    ;PAUSE BETWEEN MODE CHANGES
0681 CDA107          CALL  PAUSE
0684 CD0701          CALL  PAGE     ;CLEAR SCREEN
0687 CD1301          CALL  CHAR     ;AND FINALLY... CHANGE MODE
068A C32C06          JMP   DEM30
068D 3E01    DEM33:  MVI   A,MAXC   ;SHIFT TO MAX COLORS
068F C37F06          JMP   DEM36
0692 3E10    DEM35:  MVI   A,BLK    ;TIME TO ERASE
0694 C37206          JMP   DEM38
             ;
             ;DEMO #4: ANIMATION
             ;
0697 3E03    DEM4:   MVI   A,R64    ;BIG CHARACTERS
0699 CD1301          CALL  CHAR
069C CD0701          CALL  PAGE
069F 218028          LXI   H,2880H ;POSITION TITLE
06A2 CD0A01          CALL  CURSOR
06A5 212008          LXI   H,STR09 ;'ANIMATION'
06A8 CD9107          CALL  STRING
06AB CD1601          CALL  ANIMAT   ;SWITCH BUFFERS
06AE CD0701          CALL  PAGE     ;CLEAR OTHER BUFFER
                                    ;  (OR ERROR MESSAGE IF ONE)
06B1 218028          LXI   H,2880H ;ADD TITLE THERE TOO
06B4 CD0A01          CALL  CURSOR
06B7 212008          LXI   H,STR09
06BA CD9107          CALL  STRING
06BD 3E02            MVI   A,R128   ;NEED SOME RESOLUTION
06BF CD1301          CALL  CHAR
06C2 0604            MVI   B,TWO    ;LET THIS SINK IN
06C4 CDA107          CALL  PAUSE
06C7 211200          LXI   H,18D    ;NEED SOME TERRA FIRMA
06CA CD0A01          CALL  CURSOR
06CD 26FF            MVI   H,0FFH
06CF CD1001          CALL  LINE
06D2 CD1601          CALL  ANIMAT   ;PUT IN BOTH BUFFERS
06D5 CD0A01          CALL  CURSOR
06D8 2600            MVI   H,00H
06DA CD1001          CALL  LINE
06DD 0610            MVI   B,16D    ;STARTING POSITION
06DF CD0E07  DEM40:  CALL  MAN      ;DRAW NEW FRAME
06E2 CD1601          CALL  ANIMAT   ;TRY EVEN IF NOT SUPPORTED
06E5 3E10            MVI   A,BLK    ;ERASE OLD ONE
06E7 CD1301          CALL  CHAR
06EA 3A2C08          LDA   MAXRD    ;DOUBLE BUFFERED?
06ED E680            ANI   80H      ;TEST BIT
06EF CAF306          JZ    DEM41    ;DON'T BACK UP TO ERASE
06F2 05              DCR   B        ;BACK TO PREVIOUS FRAME
06F3 CD0E07  DEM41:  CALL  MAN      ;ALL GONE
06F6 3E17            MVI   A,WHI    ;BACK TO WHITE
06F8 CD1301          CALL  CHAR
06FB 3A2C08          LDA   MAXRD    ;DID WE DECREMENT BEFORE?
06FE E680            ANI   80H      ; WELL...
0700 CA0407          JZ    DEM42    ;NO, SO DON'T DOUBLE INCR
0703 04              INR   B        ;ADVANCE TO NEXT FRAME
0704 04      DEM42:  INR   B
0705 78              MOV   A,B
0706 FEF0            CPI   0F0H     ;DONE YET?
0708 DADF06          JC    DEM40    ;KEEP ON TRUCKING
070B C30005          JMP   DEMO     ;START ALL OVER AGAIN
             ;
             ;SUBROUTINE TO DRAW A LITTLE MAN
             ;
070E 78      MAN:    MOV   A,B      ;X IS IN B, 0 TO 255
070F E60F            ANI   0FH
0711 D608            SUI   08H      ;ARM SWING (AS)
0713 4F              MOV   C,A      ;C = AS
0714 07              RLC            ;TIMES 2
0715 57              MOV   D,A      ;  FOR LEG SWING (LS)
0716 78              MOV   A,B      ;FIND FIXED LEG
0717 E6F0            ANI   0F0H
0719 C608            ADI   08H      ;R=(X AND F0)+8
071B 5F              MOV   E,A      ;E = R
071C 78              MOV   A,B      ;L = X + LS
071D 82              ADD   D
071E 57              MOV   D,A      ;D = L
071F 78              MOV   A,B
0720 3C              INR   A        ;A = X + 1
0721 05              DCR   B        ;B = X - 1
             ;ALL SET TO DRAW ALL BUT HEAD
0722 2E14            MVI   L,20     ;START WITH LEGS
0724 63              MOV   H,E
0725 CD0A01          CALL  CURSOR   ;R, 20
0728 67              MOV   H,A
0729 2E24            MVI   L,36
072B CD1001          CALL  LINE     ;X + 1, 36 >> RT LEG
072E 60              MOV   H,B
072F CD1001          CALL  LINE     ;X-1, 36 >> HIPS
```

Listing 2 continued on page 194

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Listing 2 continued:

```
0732 62               MOV   H,D
0733 2E14             MVI   L,20
0735 CD1001           CALL  LINE     ;L, 20 >> LEFT LEG
0738 2E25             MVI   L,37     ;LEFT SIDE OF BODY
073A 67               MOV   H,A
073B CD0A01           CALL  CURSOR   ;X+1,37
073E 2E30             MVI   L,48
0740 CD1001           CALL  LINE     ;X+1,48 >> LEFT BOD
0743 2E26             MVI   L,38
0745 91               SUB   C
0746 67               MOV   H,A
0747 CD1001           CALL  LINE     ;X+1-AS, 38 >> LEFT ARM
074A 78               MOV   A,B      ;SAME FOR RIGHT SIDE
074B 67               MOV   H,A
074C 2E25             MVI   L,37
074E CD0A01           CALL  CURSOR   ;X-1, 37
0751 2E30             MVI   L,48
0753 CD1001           CALL  LINE     ;X-1, 48 >> RIGHT BOD
0756 2E26             MVI   L,38
0758 81               ADD   C
0759 67               MOV   H,A
075A CD1001           CALL  LINE     ;X-1+AS,38 >> RT ARM
075D 04               INR   B        ;FINALLY DO HEAD
075E 2E30             MVI   L,48     ;NOTE: B IS BACK TO
                                     ;   ORIGINAL VALUE = X
0760 60               MOV   H,B
0761 CD0A01           CALL  CURSOR
0764 2E34             MVI   L,52
0766 CD1001           CALL  LINE     ;X, 52 >> NECK
0769 78               MOV   A,B
076A D602             SUI   2
076C 67               MOV   H,A
076D CD1001           CALL  LINE     ;X-2, 52
0770 2E38             MVI   L,56
0772 CD1001           CALL  LINE     ;X-2, 56
0775 78               MOV   A,B
0776 C602             ADI   2
0778 67               MOV   H,A
0779 CD1001           CALL  LINE     ;X+2, 56
077C 2E34             MVI   L,52
077E CD1001           CALL  LINE     ;X+2, 52
0781 60               MOV   H,B
0782 CD1001           CALL  LINE     ;X, 52  >> END OF HEAD
0785 2E36             MVI   L,54
0787 C602             ADI   2
0789 67               MOV   H,A
078A CD0A01           CALL  CURSOR   ;X+4, 54
078D CD0D01           CALL  DOT      ;THE NOSE!
0790 C9               RET

                  ;
                  ;COMMON SUBROUTINES
                  ;
                  ;     EXCEPT AS NOTED... ALL REGISTERS ARE PRESERVED
                  ;
                  ;SUBOUTINE STRING
                  ;     DISPLAY THE STRING OF ASCII CHARACTERS POINTED
                  ;       TO BY H,L TERMINATING WITH "$".
                  ;     EXITS WITH H,L POINTING TO THE "$".
0791 F5           STRING: PUSH  PSW      ;SAVE A AND FLAGS
0792 7E           STR000: MOV   A,M      ;GET CHAR
0793 FE24                 CPI   '$'      ;TERMINATOR
0795 CA9F07               JZ    STR001
0798 CD1301               CALL  CHAR     ;OK... SO DISPLAY IT
079B 23                   INX   H        ;NEXT CHAR
079C C39207               JMP   STR000
079F F1           STR001: POP   PSW      ;RESTORE A
07A0 C9                   RET
                  ;
                  ;SUBROUTINE PAUSE
                  ;     DELAY A BIT... AS DETERMINED BY REGISTER B
                  ;     EXITS WITH B=0.
                  ;     WARNING: B = 0 IS MAX, NOT ZERO, DELAY
                  ;     SENSE SWITCHS SET TO 01H CAUSE INFINITE PAUSE
                  ;
07A1 E5           PAUSE:  PUSH  H        ;NEED A COUNT DOWN REGISTER
07A2 F5                   PUSH  PSW
07A3 210080               LXI   H,8000H  ;MAKE UNIT DELAY SHOR
07A6 2D           PAUS00: DCR   L        ;A 3 REGISTER COUNT DOWN
07A7 C2A607               JNZ   PAUS00
07AA 25                   DCR   H
07AB C2A607               JNZ   PAUS00
07AE 05                   DCR   B
07AF C2A607               JNZ   PAUS00
07B2 DBFF         PAU001: IN    0FFH     ;READ SENSE SW
07B4 3D                   DCR   A        ;ARE THEY SET TO ONE
07B5 CAB207               JZ    PAU001   ;  YES...
07B8 F1                   POP   PSW
07B9 E1                   POP   H
07BA C9                   RET
                  ;
                  ;STRING DEFINITIONS
                  ;
07BB 1742595445STR00:  DB   WHI,'BYTES$$$$$$$'
07C7 4752415048STR01:  DB   'GRAPHICS$$$$'
07D2 5354414E44STR02:  DB   'STANDARDS$$$'
07DD 174655404CSTR03:  DB   WHI,'FULL$'
07E3 11431541F14STR04: DB   RED,'C',YEL,'O',GRN,'L',CYN,'O',BLU,'R$'
07EE 1154124F13STR04G: DB   11H,'T',12H,'O',13H,'N',14H,'A',15H,'L$'
07F9 17434F4E54STR05:  DB   WHI,'CONTROL$'
0802 174C415247STR06:  DB   WHI,'LARGE',MAXR,'$'
080A 414E442053STR07:  DB   'AND SMALL',R128,'$'
0815 4348415241STR08:  DB   'CHARACTERS$'
0820 17414E494DSTR09:  DB   WHI,'ANIMATIONS'

                  ;
                  ;VARIABLE STORAGE AREA
                  ;
082B              MAXCD:  DS    1        ;MAXC DISPLAY DISCRIPTOR
082C              MAXRD:  DS    1        ;MAXR DISPLAY DISCRIPTOR
082D                      DS    100H     ;STACK
092D              STACK:  DS    1
092E                      END   DEMO
```

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A User's Look at Tiny-c

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As the microcomputer industry has responded to a rapidly growing market — a market composed of small business users and others who are less interested in computers than they are in *using* computers for particular applications — a considerable amount of good system-level software has become available. Unfortunately, any given computer hobbyist is able to use only a small portion of this software.

It is inevitable that the microprocessor that is chosen to be the central processing unit of a small computer will restrict the range of available software to the subset written for that microprocessor. But for the vast majority of computer hobbyists, there are two other impediments to using the system programs that are now on the market (assemblers, text editors and processors, language interpreters and compilers, and the like) that are far more important. First, available programs often require large amounts of memory and floppy disk storage; second, almost all of the software on the market requires that the user have a particular manufacturer's computer or, at the very least, a particular disk operating system.

There is a simple way around these two restrictions. The software vendor can sell his product as source code for particular microprocessors, with directions for adapting the program to the end user's computer system. Given the economic pressures of the software market, this has not proved to be a popular approach. However, an intriguing experiment in selling a sophisticated system program on this basis is being carried out by tiny-c associates (the lower-case style is theirs). This program offers an interpreter (for an exceedingly modest price) for the structured programming language *tiny-c* that can be easily adapted to any 8080-family or LSI-11/PDP-11 computer.

Tiny-c is based on the C programming language, which was developed at Bell Laboratories, where it was used to write the UNIX operating system under which the C compiler can be run. As might be expected of a programming language that can be used to write operating systems, C mirrors the actual operation of a computer somewhat more closely than does a language like BASIC. Tiny-c follows C's example in this respect, as well as most others. For those familiar with C (I was not at the time I started using tiny-c on my home computer), I should point out that tiny-c is not a true subset of C. There are slight syntactical differences, and tiny-c has a comparatively restricted set of statements, fundamental data structures, and operators.

Tiny-c follows C's example in another way: a significant portion of the tiny-c language system is written in tiny-c itself. The actual interpreting of tiny-c code is done by a program that is written in 8080 or PDP-11 assembly language. But tiny-c pro-

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grams are written, edited, and (in most cases) run under the supervision of a *program preparation system* that is written entirely in tiny-c. The importance of this should not be underestimated. It means that it is easy to change the way the user interacts with the tiny-c system by writing a new program preparation system in tiny-c. This new program preparation system can be tested and debugged under the old version. While any changes in the way tiny-c programs are interpreted would have to be made as alterations to the assembly language code, the type of customizing that most users will probably be interested in can be done without reassembly. For the truly ambitious, the source code for the interpreter is available for alteration, substitution, or just general tinkering.

The Language

Before looking at the system in more detail, a description of the language is in order. Tiny-c is quite unlike BASIC. There are no line numbers. Variables can have names of any length (although only the first seven and last one letters of a variable or function name are actually used by the interpreter). Control flow is not limited to a sequence of individual

Tiny-c Program Example

Listing 1 is a tiny-c function to fill a buffer with ASCII text, such as might be required in a text processing program. The program fragment illustrates a number of features of tiny-c.

Buffer, cursor, and blockend are all global variables, which must be declared outside any function. Buffer is a pointer to an address in computer memory representing the start of the buffer. Cursor is a pointer to the address of the next byte of text to be printed. Blockend is a pointer to the address following the last byte of text that has been read from an external file; new text will be placed beginning at blockend.

The first two lines of the function declare local variables. Record count is an integer variable. Pointer is a character pointer, which will later be set to an address within the buffer. The byte it will point to is pointer(0).

In the third line of the function, a standard library function called movebl is called. Movebl will shift any text that is left over from the previous file record to the start of the buffer. Its arguments are a pointer to the first character to be moved, a pointer to the last character to be moved, and the distance to move the block (in this case, the negative distance represented by buffer-cursor).

Once the leftover text has been moved, the cursor and blockend pointers must be reset. The blockend pointer is moved back the same distance that the entire block was moved. In the same statement, the local pointer is set to the same address. Accomplishing the same setback, but somewhat more simply, the address of cursor is assigned the address of the start of the buffer.

The parentheses in the sixth line of the function set the order of evaluation inside the condition of the if statement. First, another standard library function, fread, is called to read a new record from the file. Fread's arguments are a pointer to the address showing where to place the new text (blockend), and a unit number designating the mass storage device. Fread returns the number of bytes actually read, if any, or a negative number indicating that the end of the file has been reached (the end-of-file record, by convention, contains no data). The local variable recordcount is set to the number of bytes read.

The statement subject to the if condition, enclosed in brackets, will be executed only if recordcount is positive (ie: if the record read contains new text). If it is, the condition is fulfilled and the code that is enclosed in the brackets is executed. First the blockend pointer is moved up to the end of the new text. Then a while loop is used to excise any carriage returns in the text (tiny-c files as implemented in my system do not contain separate line feeds). Note how the byte pointer(0) can be evaluated as either an ASCII integer code (13 = carriage return) or a character (' ', or blank). Note also how the local pointer is incremented through the new text. When it reaches the address of blockend, the while condition fails and the loop is terminated. As it so happens, this is also the end of the if statement, hence the two successive closing brackets.

Now all that is left is to return control to the calling function. The return statement is entirely optional; one final bracket will do the job. But the calling function may need to know how many bytes have been placed in the buffer, so recordcount is returned. Recordcount becomes the numerical value of the function fillbuffer to the calling function. Fillbuffer could therefore be used to represent an integer in some tiny-c expression.

```
fillbuffer [
    int recordcount
    char pointer(0)
    movebl (cursor, blockend, (buffer - cursor))
    pointer = blockend = blockend + (buffer - cursor)
    cursor = buffer
    if ((recordcount = fread (blockend, 1)) > 0) [
        blockend = blockend + recordcount
        while (pointer < blockend) [
            if (pointer(0) = 13) pointer(0) = ' '
            pointer = pointer + 1
        ]
    ]
    return recordcount
]
```

Listing 1

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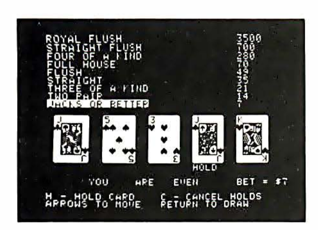
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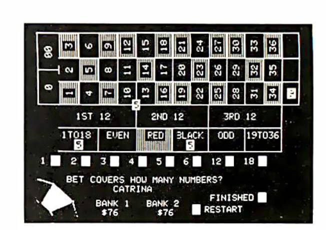
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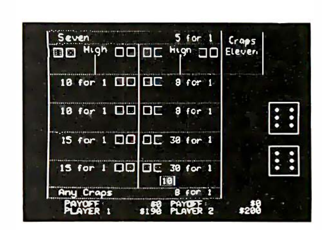
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statements, as is the case in BASIC, but includes the invocation of functions (the equivalent in this context to BASIC subroutines), either through explicit calls to a given function, or by using the function as an element in a more complex tiny-c expression.

All tiny-c programs are composed of functions. Tiny-c functions, in turn, are composed of other functions, tiny-c statements, and operators. The list of tiny-c statements is small but surprisingly flexible. It includes *if*, *if-else*, *while*, *return* (which provides an optional way for returning some computed value of a function to the calling function), and *break* (which terminates the innermost current *while* loop prematurely, ie: without waiting for the normal termination condition to be met).

There is no explicit "do" statement. Tiny-c functions are called directly by simply placing their names in the program text. They are invoked indirectly by their use as elements in a larger tiny-c expression. Within a logical expression, tiny-c functions take on whatever value the function returns, although a function is not required to return any value at all (the default is zero). A series of function calls, or any other series of tiny-c statements, can be turned into a compound statement and executed as a unit by enclosing it in brackets.

Tiny-c operators include unary minus (−), multiplication (*), integer division (/), remainder following division (%), addition (+), subtraction (−), less than (<), greater than (>), less than or equal (< =), equal (= =), not equal (!=), greater than or equal (> =), and assignment (=). Choosing the *single* equal (=) sign for assignment and the *double* equal (= =) for testing equality may seem rather odd at first, as does the choice of !=, instead of the more common <>, as the inequality operator. In practice, both choices are easy to adapt to and soon become intuitive.

The number of primitive tiny-c data structures, like the number of statements and operators, has been kept to a minimum. There are two fundamental types of data in tiny-c: 16-bit signed *integers* (which permits numbers from −32768 to 32767), and 8-bit *characters* (which can actually represent any 8-bit quantity). These two basic structures can be combined into arrays, but tiny-c does not provide any way to deal with arrays as a single entity; this must be done with functions. You cannot, for example, write [if (answer == "Yes") then startgameover] in tiny-c because the character array "Yes" cannot be compared with anything using the equality operator. Instead you must write a function to perform a letter by letter comparison.

In addition to integers, characters, integer arrays, and character arrays, more complex data structures representing any combination of the fundamental structures can be created. On the other hand, tiny-c does not provide services to create or process these more complex data structures in the manner of the Pascal language. These must be developed and accessed by specific functions through the use of pointers, which provide an essentially convenient but rather low-level way of searching through memory.

Pointers are declared in tiny-c

through the declaration of an array. An array is declared by declaring its *type* (integer or character) and its *last element.* All arrays begin with element 0, so the tiny-c declaration [int arrayofintegers(10)] creates an 11-element array of integers (2-byte values), and the declaration [char arrayofcharacters(10)] creates an 11-element array of single-byte values.

In either case, the pointer is simply the array name without a subscript. Therefore, the above integer declaration has simultaneously declared a pointer, arrayofintegers, which can be aimed at the start of any 2-byte value in the array by moving it, through a tiny-c expression, in 2-byte increments. The pointer, which is aimed at the zeroth element of the array at the time of declaration, can therefore be moved to the third element (the start of the third 2-byte integer) by setting [arrayofintegers = arrayofintegers + 3] without any requirement of capturing the data in the intervening two elements of the array. Similarly, the pointer arrayofcharacters can be moved in 1-byte increments. There is no way to declare a pointer without declaring at least one element of an array, so when the array itself is not needed (eg: when the pointer is going to be used to keep track of data in a preexisting array such as a buffer), the tiny-c convention is to declare an array whose last element is 0.

This ability to declare pointers and move them around at will makes it possible to use tiny-c pointers to address any location in the computer's available memory. The addressing is, of course, relative to where the tiny-c interpreter decides to locate the first element of the array, but with a few lines of assembly language code it is possible to add the absolute addressing that many BASIC interpreters provide through PEEK and POKE commands.

Tiny-c is quite permissive about interchanging integer and character data, thus permitting reference to characters by their numerical ASCII codes. It also provides a powerful facility for generating interesting and often complex program bugs.

It should be fairly obvious that tiny-c is not a very sophisticated language, and there are certainly features that I miss. Boolean operators would be handy, as would multiple-precision integer and floating-point arithmetic. I don't particularly miss the rather wide variety of mathematical functions that are provided as part of my BASIC interpreter, and I can duplicate the very useful string-handling functions that are available in BASIC by either writing them in tiny-c or by adding machine language subroutines to the tiny-c system as described below.

The most important feature of tiny-c is one that is essentially unavailable in BASIC. This feature is the ability to create functions and then use or manipulate them without further thought as to what is inside. Tiny-c functions exist as independent worlds of their own. They have their own local variables, although it is also possible to define global variables and have all functions access them. They can accept arguments and manipulate them within the function, without changing the value that was passed by the calling function. In

fact, a tiny-c function is *not* able to change the value of a variable that is passed to it (except internally) *unless* an express provision is made.

This reliance on functions as fundamental building blocks of programs has three important consequences:

- Programs are easy to read. They are not only modular, but because control flow is altered only by the invocation of other tiny-c functions or the intervention of a few simple tiny-c statements, it is easy to follow what the program is doing. Combining this with the availability of long, descriptive variable and function names makes it possible to read tiny-c programs in a way that is almost as close to reading English text as it is to reading a program written in BASIC or FORTRAN.

- Programs are easy to alter. Since functions are atomic units as far as other functions are concerned, it is possible to change or substitute a function without worrying about unanticipated effects of the change on other parts of the program. Obviously, it is not possible to change a data structure used by other functions without ill effects, or blithely alter global variables (which are therefore best kept to a minimum). It is possible to rewrite a function to make it more efficient or to add a strictly local feature without resulting in the blowup of some other function.

- Tiny-c functions can be kept in a library, taken out in the future, and used in new programs. With a little care, it is possible to write a function in a way that maximizes its generality and its future utility. In many instances, it is convenient to think of previously written tiny-c functions, not simply as potential components of new programs, but as extensions to the language. The program preparation system and the machine language interface provided in the tiny-c system encourage this, so perhaps it is time to describe the system in detail.

The System

The program preparation system and the machine language interface are two of the six main parts of the tiny-c system. The others are the interpreter itself, a library of commonly used tiny-c functions, a library of special purpose functions that have been coded in machine language to increase execution speed, a set of input and output routines to service a console terminal and a mass storage device, which must be coded by the user for his own installation.

Everything except the I/O (input/output) routines is provided in source-code form (8080 or PDP-11 assembly language, or tiny-c) in the *tiny-c owners manual*, which is available from tiny-c associates, POB 269, Holmdel NJ 07733, and currently sells for $40. The programs are also available on various machine-readable media in a number of formats. The one used by my computer, a Heath H8 with cassette mass storage, is not one of these, so I rather laboriously typed in the entire 8080 source code. Fortunately, the listings in the *tiny-c owner's manual* are quite legibly printed.

The interpreter is quite compact. Including the library of special functions that are coded in machine language and loaded along with it, the interpreter occupies a scant 4244 bytes in my system. There is no limitation on recursion (functions calling themselves, either directly or indirectly, where the function calls another function which calls the original calling function). But memory allocation is static. So, for example, a program that uses an unusually large number of active variables at one time might conceivably not run, even though plenty of extra memory was available in the section allocated for the program text. This would require that you stop the interpreter and reallocate memory. In practice, I have yet to have this happen. The internal operation of the interpreter is described in considerable detail in a chapter of the *tiny-c owner's manual*, which should facilitate making alterations.

I was slightly disappointed with the speed of execution of tiny-c. It is difficult to make comparisons with BASIC, mainly because the languages are so dissimilar, but also because my BASIC interpreter includes a large number of functions that speed up program execution considerably. Many of these functions, such as string handling functions, could be added to tiny-c as machine language subroutines, so any comparison that relies on the use of these special purpose BASIC functions is somewhat unfair. Still, when running through a



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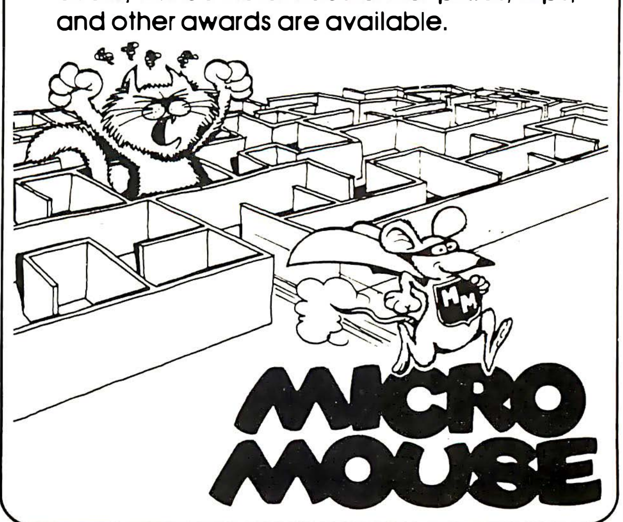
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loop of simple variable assignments, tiny-c seemed to operate only a third as fast as my BASIC interpreter.

Functions in Machine Language

The machine language functions supplied with tiny-c perform a variety of tasks. One moves blocks of data around in memory, another counts the number of occurrences of a given character within a memory field, still others interface between tiny-c and the input/output routines supplied by the user. The user can add to this so-called "standard library" of machine language functions. Tiny-c provides several utility routines which are available to user-coded functions. These simplify the interface between tiny-c and machine language.

One thoughtful feature is a set of special calls to external subroutines which take place (if enabled) at the beginning of any program, at the start of every tiny-c statement within a program, and when the program finishes running. The manual suggests that these may be used to create a *debugger*, which could allow you to single-step through a tiny-c program, set breakpoints, or enable a *profiler* which could count how often each statement is executed.

Functions in tiny-c

Aside from the standard library of machine language functions, there is a standard library of functions coded in tiny-c. These are normally loaded with the program preparation system. Like the machine language functions, this standard library of tiny-c functions is a mixed bag. Some just dress up machine language functions (which are called by number) with a descriptive name. Others convert from ASCII to binary and vice versa, read and write strings to the console terminal, and load and dump files. Continuing the parallel with the machine language functions, the user can add his own functions to the tiny-c library. This provides a convenient way to store functions that are used often at a given installation (eg: a function to drive a special device, such as a digital plotter).

Program Preparation System

The program peparation system is the part of the tiny-c system that the user is most conscious of, because it mediates most interactions with the interpreter. As an editor, the program preparation system is quite adequate, but unexceptional. It provides commands for inserting text, moving a given number of lines up or down, locating a given line by number (tiny-c does not use line numbers, but the editor keeps count for its own purposes), locating a given string (the user may optionally specify whether the string being searched for is at the beginning or the end of a line), editing strings within a line, deleting lines, and reading and writing files (program text, plain text, or data). The one drawback to its being written in tiny-c is that the editor operates a bit slowly, but not so slowly as to be frustrating.

The program preparation system also permits you to execute any tiny-c function that is in the standard library or entered as program text. This means it is possible to run any program under the editor. For those who have floppy disks, that is not a particularly important advantage. For those, like myself, who depend on cassettes for mass storage, the freedom from having to shuttle programs in and out of memory is a big plus. The fact that the editor can be used to run a program also means that tiny-c, like BASIC, has a single operating environment. Programs can be written, tested, debugged, and run without the user having to consciously switch from one mode to another.

The program preparation system is entirely optional. It is provided in two forms. One is neatly formatted and commented, and occupies about 9000 bytes. The other is "crunched" — stripped of all of its unnecessary indentations and spaces. Because tiny-c is essentially free-form, this has no effect on program function. However, it renders the "crunched" code relatively unreadable. The saving is about 5000 bytes which, for a program that resides in memory for the amount of time that program preparation system does, is a fair trade for legibility.

Programs which do not use the

program preparation system (ie: those that operate directly under the interpreter) must begin execution with a function named "main." Other than that, any program that will operate under the program preparation system will operate directly under the interpreter, although the library functions normally loaded along with the program preparation system will probably have to be loaded with other programs.

By dispensing with the amenities provided by the program preparation system, a given system can run a tiny-c program that is roughly 5000 bytes longer than it could otherwise accept. With 24 K bytes of memory available on my system, I have approximately 8 K bytes of program space with everything loaded: the interpreter, a standard console driver, my I/O interface routines, and the program preparation system. One very useful improvement would be to provide text compression that would permit a series of spaces (which should be used liberally in a language like tiny-c for indenting) to be packed into a single byte. This, however, would require some changes to the interpreter.

Support Services

Before moving on to a brief description of the procedures for installing tiny-c, I should say a few words about the quality of the documentation and support for the tiny-c system. This is a rather low-priced item, but that fact is not reflected in the *tiny-c owner's manual*. The manual is slickly produced. As noted before, the quality of the printing is excellent. Comments in the assembly language code are a bit sparse, but the section on the internal operation of the interpreter explains each routine's purpose in acceptable detail. Since I was keystroking the entire source code anyway, I used the opportunity to merge in some of the documentation from the owner's manual text.

The manual provides a detailed description of the language, an operating guide to the program preparation system, several program examples along with comments on their style, the section on the internal operation of the interpreter, explicit installation instructions, and the various source codes. And it is written in coherent English.

Support is principally provided through an occasional newsletter which provides fixes for program bugs, suggested improvements, and answers to commonly asked questions. When I found a minor bug in the way that the interpreter passed arguments between functions, my letter to tiny-c associates prompted a quick acknowledgement from author Tom Gibson, although he had no immediate solution.

Installation

As noted above, the user is required to code several installation routines. These provide an interface between the computer's operating system and tiny-c. The routines write a single character to a console terminal, read a single character from the terminal, check to see if a character has been input, open files for reading from or writing to a mass storage device (such as a cassette recorder or floppy disk), read and write single records, and close files when the reading or writing is done.

Many of these functions are likely to be already available in the computer's operating system. In some

cases, the tiny-c interface will consist of nothing more than juggling the data left in particular registers to match up the requirements of the tiny-c interpreter and the operating system. In other cases, certain functions of the operating system may have to be substantially adapted to meet the specifications set out in the *tiny-c owner's manual*. Some users may have to write all of the input and output routines from scratch.

The user has a lot of latitude in designing the interface. He can simply meet the minimum specifications in the manual, or he can add features that will take advantage of the particular characteristics of his computer. In my case, I decided that I wanted to have a visual indication of all magnetic tape operations on the H8's front panel (a very useful feature of Heath's system). The interface provides that function on its own, without any intervention from the tiny-c interpreter.

While the installation instructions are quite explicit, coding the input and output routines is not a trivial task. Nevertheless, it should be well within the competence of anyone with more than nominal experience in writing programs in assembly language, as long as the programmer is familiar with the internal functioning of the computer's operating system. A few "load and go" versions of tiny-c are available for specific computers, but many users will have to provide their own interface routines. While it may not seem like a particularly interesting chore, this is what gives tiny-c its generality, thus making it available for use on a large number of computer systems.

Once the interface routines are ready, the various components of the tiny-c system are loaded and linked. A program is provided in the manual for relocating the interpreter if the address supplied (hexadecimal 2000) is unacceptable. If you have typed in all of the source code, as I did, you can assemble the interpreter anywhere you want. Those users who buy machine-readable media can load the program preparation system as easily as the other parts of the system. In my case, the editor I used to enter the program preparation source code used a format that would have been indigestible to the tiny-c interpreter, so I had to write still another routine to reformat the file. Subsequent versions of the program preparation system are written under itself, so the problem only arose once.

I had a little trouble getting tiny-c up and running the first time, but all of the problems were my own. Most, as is usually the case, were the result of inattentive reading of the manual. They were all, fortunately, easy to correct. The entire project, from first reading of the manual through writing the interface routines through keystroking the source code through debugging, took most of my spare time for about three weeks.

There is something to be said for tackling a software project of this magnitude, even if most of the real work has been done by someone else. Although I would have undoubtably bought tiny-c in machine-readable form if it had been available for my computer, the work I did during the installation gave me a much better understanding of the way the software works. That, in turn, has reduced the sense of intimidation that I have felt in dealing with programs that are this large and this complex. ■

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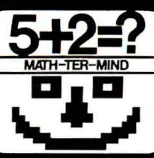
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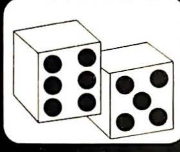
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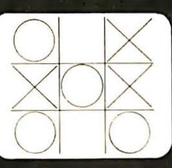
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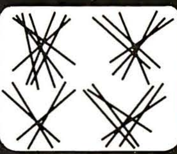
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Clubs and Newsletters

International Computer Chess Association (ICCA)

The ICCA prints two newsletters a year about ICCA planned activities, future events of interest to its members, reviews of books or articles, interesting anecdotes, and short technical papers. The ICCA is considering establishing an international archive for organizing and storing materials on computer chess, and would be interested in hearing from potential donors of funds and materials. Membership is $10 for one year. For more information, write to Professor B Mittman, Editor, *ICCA Newsletter*, Vogelback Computing Ctr, Northwestern University, Evanston IL 60201.

Washington Apple Pi

Washington Apple Pi, a group of Apple II owners and users, meets at George Washington University, Room 206, Tompkins Hall, 23rd and H St NW, Washington DC at 9:30 AM the fourth Saturday of each month. The meetings include discussions of available software, classes on assembly language, demonstrations and explanations of home-built and commercially available hardware, and they have had a discussion of the Apple II in Europe from a visiting Belgian owner. The group also publishes a monthly newsletter. For more information, write Washington Apple Pi, POB 34511, Washington DC 20034.

Central Ohio Apple Computer Hobbyists (COACH)

Meetings are on the third Saturday of each month from 1 to 5 PM. For more information, contact Tom Mimlitch, 1547 Cunard Rd, Columbus OH 43227, or phone (614) 237-3380.

New Canadian Apple Users Group

The Apples British Columbia Computer Society, #101-2044 W Third Ave, Vancouver British Columbia CANADA V6J 1L5, meets on the first Wednesday of every month. Dues are $15 per year.

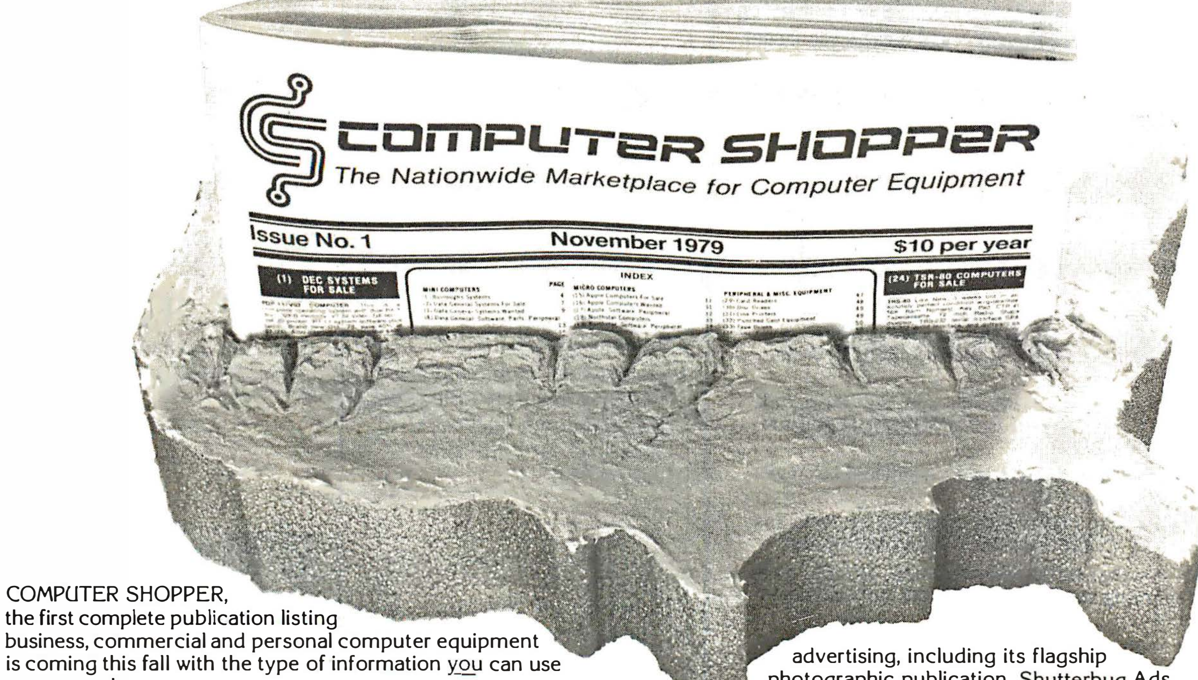
REDUCE Newsletter

The Symbolic Computation Group of the University of Utah publishes a quarterly newsletter devoted to REDUCE, a LISP-based computer algebra system designed for a variety of large computers. The newsletter is available from the University of Utah computer science department for $100. For more information, contact the Department of Computer Science, University of Utah, Salt Lake City UT 84112.

Heath Users Group (HUG)

HUG Northshore is a computer club for Heathkit computer users (H8, H11, ET3400). The club provides a forum for exchanging ideas, programs and knowledge, with the intent of developing the full potential of the computer system. The club meets the second Wednesday of each month at 7 PM at the following address: Hill Tech Building, 88 Holten St, Danvers MA 01923. For a free copy of their monthly newsletter, write HUG Northshore, POB 112, Danvers MA 01923.

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PCIR is a monthly report on personal computing in business, professional, educational, hobby and home applications. The newsletter covers such topics as the market for board-level microcomputers including market shares and trends, reviews of popular microcomputer systems, the status of computer retail stores, and other items of general interest. *PCIR* is available from Vantage Research Inc, 2680 Bayshore Rd, Mountain View CA 94043, for $195 for one year.

Appleseed Newsletter

Appleseed Newsletter, c/o The Computer Shop, 6812 San Pedro, San Antonio TX 78216, covers the current and future events of this Apple users group's meetings, which center around swapping programs, discussions and the use of new products.

Sorcerer User's Newsletter (SUN)

Sorcerer User's Newsletter is published monthly by Steven J Long, 792 Laurie Ave, Santa Clara CA 95050. Included are short programs sent by users, notes on problems or fixes, comments on accessories, and anything else which is of general interest to Sorcerer users. A program library is available for use by subscribers. The subscription rate is $10 per calendar year.

A New Apple Users Group

There is a new users group in New York City: The Big Apple User Group, 55 Water St, c/o Bruce Brewster, Drysdale Securities, New York NY 10004. For more information, contact Tony Cerreta, (914) 636-3417 or write to the above address. ■

BYTE's Bugs

Redundancy Rules These Pages...

Readers may have noted some redundancy in text on pages 8 and 10 of the November 1979 BYTE. As Murphy would have it, this was discovered in the final printed versions of BYTE, as opposed to the more typical discovery of such effects in the "blue line" proof copies we get of each issue. So, rest assured—if the paragraph beginning on page 10 looks familiar when you read it, it is indeed an inadvertent repeat of an incomplete paragraph at the bottom of page 8....CH

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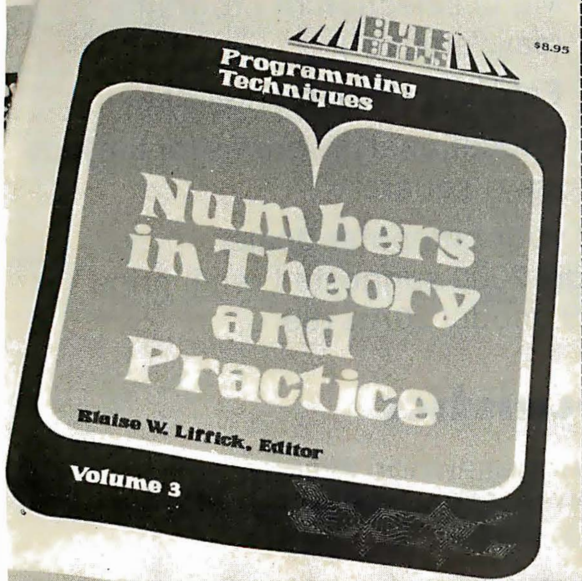
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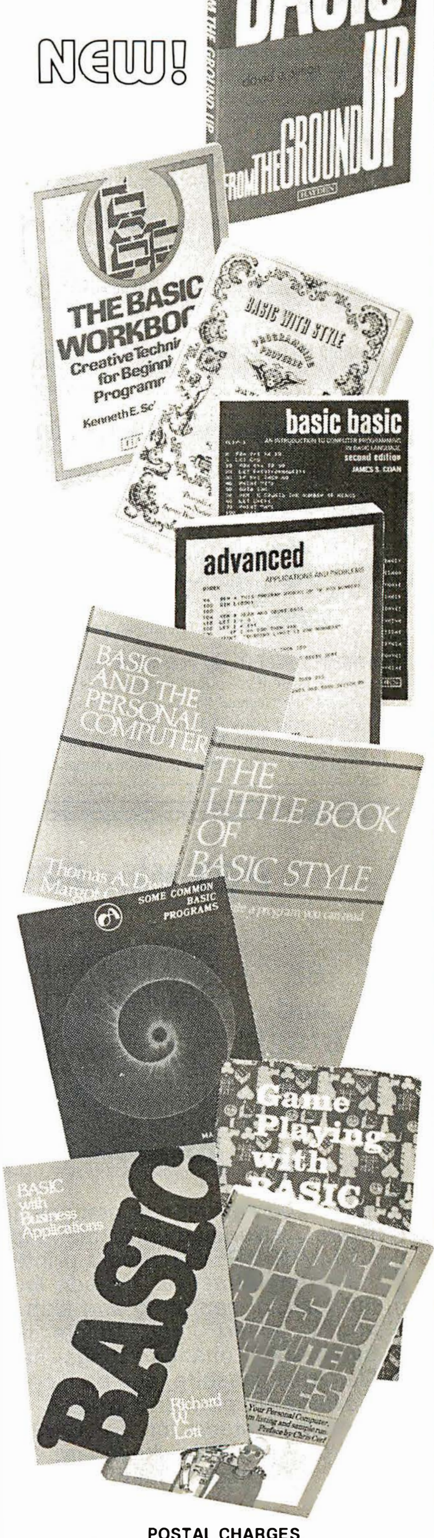
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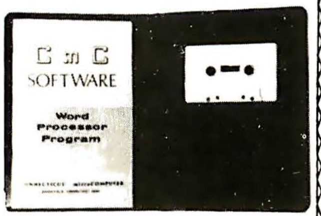
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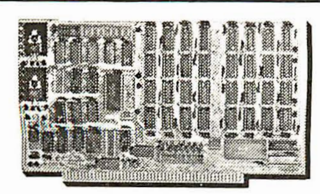
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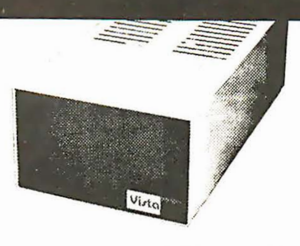
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Some Notes on Modular Assembly Programming

James Lewis
Micro Logic Corp
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James Lewis is president of Micro Logic Corp, a microcomputer application firm involved in microprocessor applications ranging from LASER beam controllers to office systems.

Despite the dominance of BASIC over machine code (eg: assembly language) in the programming of personal microcomputers, a significant number of programs are written in machine code, and for many good reasons: machine programs usually run much faster than BASIC programs; machine coded programs do not require the overhead in memory space taken up by a BASIC interpreter; they often take less space than equivalent BASIC programs; and a BASIC interpreter may not be available on a given system.

The purpose here is not to further compare BASIC with machine code but rather to discuss a good way to use machine code, given that it has been selected as the language of choice. The method to be described focuses on an important aspect of machine coding: the use of subroutines.

Example

The technique is best explained and illustrated with an example. Although 8080 code will be used (and regardless of whether or not the reader is familiar with 8080 machine code), the overall philosophy applies to other machines. The problem is to write a program that generates pseudorandom notes of music through a DAC (digital to analog converter). Incidentally, the example was implemented on a TRS-80 using a TRS-80-DAC board.

The Algorithm

The algorithm chosen to produce pseudorandom music is as follows:

1. Generate a pseudorandom number;
2. Initialize a cycle count to 32;
3. Initialize note value of 16 mV;
4. Count down from the pseudorandom number to 0 to produce a delay;
5. Output the voltage;
6. Multiply the voltage by −1;
7. Decrement the cycle count and go to 4 if not 0;
8. Return to the monitor if the shift key is down;
9. Otherwise go to 1.

This will produce random notes, each consisting of 32 square wave transitions and a voltage swing of +16 mV to −16 mV until the shift key is pressed to abort the program.

Listing 1: Nonmodular code for pseudorandom tone generator.

```
START   MVI   B,1       B = RUNNING RANDOM TOTAL
        MVI   C,16      C = DAC VOLTAGE
        MVI   D,32      D = CYCLE COUNT FOR A NOTE
LOOP1   MOV   A,B       A = LAST RANDOM NUMBER
        ADI   187       A = NEW RANDOM NUMBER
        MOV   B,A       B = NEW RANDOM NUMBER
        MOV   E,D       E = CYCLE COUNT FOR A NOTE
LOOP2   MOV   A,B       A = NEW RANDOM NUMBER
DLY     DCR   A         PRODUCE A DELAY BY COUNTING
        JNZ   DLY       DOWN FROM THE RANDOM NUMBER
        MOV   A,C       A = DAC VOLTAGE
        OUT   DPORT     SET DAC VOLTAGE
        CMA             MULTIPLY BY −1 BY TAKING
        INR   A         THE 2'S COMPLEMENT
        MOV   C,A       C = NEW DAC VOLTAGE
        DCR   E         DECREMENT CYCLE COUNT
        JNZ   LOOP2     LOOP IF NOT 0
        LDA   SHKEY     A = VALUE OF SHIFT KEY
        ORA   A         TEST A
        JZ    LOOP1     NEXT NOTE IF NOT PRESSED
        JMP   MONITOR   ELSE RETURN TO MONITOR
```

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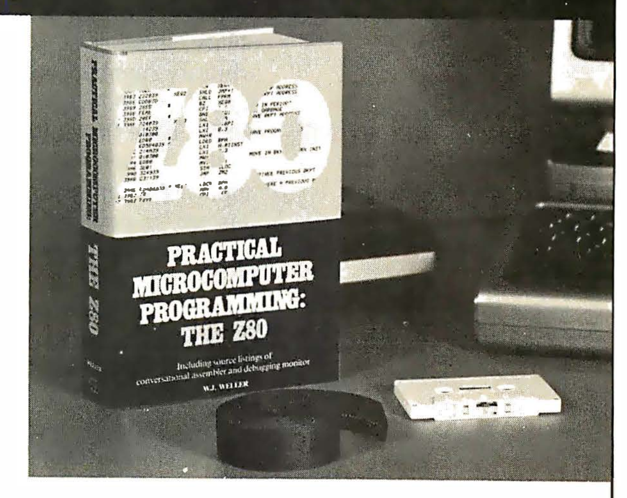
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Nonmodular Code

Listing 1 is the 8080 implementation of the above algorithm without using the modular machine code practice. For simplicity, the trivial algorithm of adding an arbitrary number like 187 to a running total is used to produce pseudorandom numbers.

The code first initializes some parameters. It then generates a simple pseudorandom number. After setting up a cycle count, it sets up a pseudorandom delay count and then executes the pseudorandom delay. It then outputs and inverts the note value, decrements the count, and loops if necessary. Next it checks for a user abort with the shift key and either loops or goes to the monitor.

This style of coding has many disadvantages over the modular style given in listing 2. It is relatively hard to follow, hard to explain, and hard to change. Compare it with the modular approach for yourself.

Listing 2: Modular code for pseudorandom tone generator. This form is better than the nonmodular form because each of the subroutines can be accessed separately and debugged more easily.

```
START    CALL  RANDOM    A = RANDOM NUMBER
         CALL  NOTE      GENERATE NOTE USING (A) AS FREQUENCY
         CALL  ABORT     ABORT TO MONITOR IF SHIFT KEY DOWN
         JMP   START     LOOP FOR NEXT NOTE

RANDOM   LDA   RANUM     A = OLD RANDOM NUMBER
         ADI   187       A = NEW RANDOM NUMBER
         STA   RANUM     SAVE NEW RANDOM NUMBER
         RET             RETURN TO CALLING PROGRAM
RANUM    DATA  1         INITIAL RANDOM NUMBER

NOTE     PUSH  B         SAVE B REGISTER VALUE
         MVI   B,32      B = 32 FOR CYCLE COUNT
LOOPN    CALL  DELAY     DELAY ACCORDING TO (A) REGISTER
         CALL  TOGGLE    FLIP DAC FOR SQUARE WAVE
         DCR   B         DECREMENT CYCLE COUNT
         JNZ   LOOPN     LOOP IF NOT 0
         POP   B         RESTORE B REGISTER VALUE
         RET             RETURN

DELAY    PUSH  PSW       SAVE THE (A) REGISTER
LOOPD    DCR   A         DECREMENT (A)
         JNZ   LOOPD     LOOP IF NOT 0
         POP   PSW       RESTORE THE (A) REGISTER
         RET

TOGGLE   PUSH  PSW       SAVE THE (A) REGISTER
         LDA   VOLTAGE   A = CURRENT VOLTAGE
         CMA             MULTIPLY BY -1 BY TAKING
         INR   A         THE 2'S COMPLEMENT
         STA   VOLTAGE   SAVE NEW VOLTAGE
         OUT   DPORT     OUTPUT VOLTAGE TO DAC
         POP   PSW       RESTORE THE (A) REGISTER
         RET             GO BACK
VOLTAGE  DATA  16        INITIAL VOLTAGE VALUE

ABORT    LDA   SHKEY     A = VALUE OF SHIFT KEY
         ORA   A         TEST VALUE
         JNZ   MONITOR   GO TO MONITOR IF PRESSED
         RET             ELSE RETURN
```

The Modular Code

We now show a different approach to the coding of the same program. Even though the code that generates the pseudorandom number is only three lines, we will make a subroutine out of it called RANDOM. We will also transform the 2 line DLY loop into a subroutine called DELAY and create a subroutine called TOGGLE to invert the note value. A subroutine can also be set up to generate a note given a delay value called NOTE, which will call DELAY. Lastly we create a routine to check for a shift key abort called ABORT.

The result of modularizing the program in this way yields several advantages. Each of the subroutines is easily understood because of its simplicity, and will be useful, without changes, in more complex music synthesis programs and in unrelated programs. The code is easier to debug and modify. To be fair, it should be pointed out that the modular code in this case is longer and a bit slower. However these disadvantages are of little concern in this case; in fact, in more complex programs, the modular approach usually produces shorter code than the nonmodular approach. Lastly, an important advantage of the modular style is a simplified main routine.

The main routine, START, is significantly easier to understand and modify than the original nonmodular version. Of course we still have to write the subroutines, but each one is so small that it will be simple to code.

The RANDOM routine is simple and, since it is in modular form rather than part of some nonmodular code, it can be used by other programs or extensions of the music program given here. (Actually it is a poor pseudorandom number generator, but the point of modularization still applies.)

The NOTE routine generates a note with frequency determined by the value of A. (Actually, A gives the period, but everything is random, anyway.) The NOTE routine uses both the TOGGLE and DELAY subroutines.

Although the NOTE routine is not completely general (eg: cycle count is fixed), it can be used in programs other than the random note generator. The DELAY routine which NOTE calls is also straightforward. It is applicable to numerous situations — wherever a short variable delay is needed. The next routine toggles the note value and outputs a voltage to produce the square wave. Lastly, ABORT finishes the program. This completes the modular implementation of the pseudorandom note generator program.

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Method Comparison

Note that the modular approach has generated several useful routines that can be used in either more complex music programs or even totally unrelated programs. This applies to every routine except the main routine, which is specific to the current application. Furthermore the main routine is easy to follow and hence modify. If one wanted to create, say, a melody generator, it would be a much easier task to do so with the subroutines than the nonmodular program. In some applications the increased size of the modular code would not be outweighed by the other advantages, but in larger systems the modular approach usually generates less code. The modular version is also a little slower, but this is often of little concern.

Conclusion

The technique of breaking a machine language program down into very small logical subroutines yields numerous advantages and few disadvantages. It takes some practice to learn how to do this effectively and to see the benefits firsthand, but it is well worth the initial added effort.■

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Event Queue

In order to gain optimum coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, 70 Main St, Peterborough NH 03458. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

DECEMBER 1979

December

WPI Programs, WPI is holding two-day courses in management skills for engineering and research and design supervisors; managing under pressure; energy conservation management;and management planning, scheduling and control.

For more information, contact Worcester Polytechnic Institute, Worcester MA 01609.

December

Computer Management in the 80s. Computer Power Management Corp, POB 1403, Rockville MD 20850, is giving one- and two-day seminars on computer mangement for executives. The courses cover data processing, word processing and printing, the role of data communications in data processing, and planning and supervising automated facilities and operations. The courses will be held in major cities in the US.

December

Yourdon Seminars. Yourdon Inc, 1133 Avenue of the Americas, New York NY 10036, is offering a series of seminars on software engineering, structure design and programming for microprocessors, data base modeling and design, programming in COBOL, and data base administration, throughout cities in the US during December.

December

Datapro Seminars, Datapro Research Corp, 1805 Underwood Blvd, Delran NJ 08075, is holding various seminars covering such topics as data communication, distributed systems, data processing, word processing, minicomputers and small business computers, and more. The seminars will be held in major cities around the US. They are two-day courses.

December 2-6

MUSE North American Annual Meeting, Bahia Mar Hotel and Yachting Center, Ft Lauderdale FL. This conference of Modcomp Users Exchange (MUSE) will feature technical sessions, workshops and user/manufacturer interface sessions on the use of Modcomp computers and their related software. Contact Kathy Black, MUSE, 4620 W Commercial Blvd, Suite 6C, Tamarac FL 33319.

December 3-5

Winter Simulation Conference, Holiday Inn, Em-

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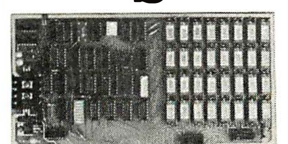
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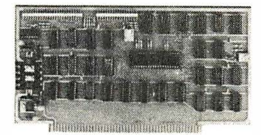
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barcadero, San Diego CA. This conference will feature papers and panel discussions on discrete and combined (discrete and continuous) simulations. Contact Professor Robert E Shannon, University of Alabama in Huntsville, School of Science and Engineering, POB 1247, Huntsville AL 35807.

December 3-5

Crime by Computer, San Francisco CA. The seminar will address the following topics of what is becoming a leading crime category: computer crime methods, changing nature of business crime, the computer criminal, vulnerability, security techniques, principles of safeguard, and the auditor's role and tools.

For more information, contact Infotech International Inc, 234 E Colorado Blvd, Pasadena CA 91101.

December 3-5

The Application of Computer Technology to Accounting Systems, Washington DC. The theme of the conference is "Information Systems as a Management Tool for the Financial Executive." The conference is sponsored by the Association of Government Accountants (AGA). Contact Ken Burroughs, DBD Systems Inc, 1500 N Beauregard St, Alexandria VA 22311.

December 3-5

Implementing Cryptography in Data Processing and Communications Systems, New York NY. Going beyond an introduction to cryptographic systems, the seminar will stress implementation of the DES and address public key implementation considerations. Contact Ms Jansen, Cryptotech, 12 Station Rd, Bellport NY 11713, (516) 286-2626.

December 3-5

COMDEX '79, MGM Grand Hotel, Las Vegas NV. This conference and exposition for third-party sellers of computer systems, word processing systems, peripherals, software packages, and media will focus on solutions to business problems normally encountered in structuring a successful dealership and the operational aspects of the dealership from both the supplier and customer's side. Contact The Interface Group, 160 Speen St, Framingham MA 01701.

December 3-7

Pascal Programming for Mini and Microcomputers, Holiday Inn, Palo Alto CA. This course covers a general approach to the use of high-level languages in small computers, including an intensive course in Pascal programming, a preview of ADA (the evolving Department of Defense standard real-time language), and an introduction to structured programming techniques.

For additional information, contact the Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton MA 02158.

December 4-6

Understanding and Using Computer Graphics, New York NY. Computer users in business or engineering firms are invited to this conference covering computer graphics, data processing, systems analysis and design, financial management and analysis, and more. Contact Frost and Sullivan, Dept C-2 106 Fulton St, New York NY 10038.

December 8-9

Data Processing for Business People, Cherry Hill Inn, Cherry Hill NJ. Management Information Corp presents this seminar to meet the needs of company management in understanding computers. The seminar includes basic concepts of data processing, alternatives (service bureaus, time-sharing), small business computer systems, program packages availability and selection, managing the computer system, and the future of data processing. Contact Management Information Corp, 140 Barclay Ctr, Cherry Hill NJ 08034.

December 10-11 and December 13-14

New York NY and Washington DC, respectively, **New User Documentation Workshops.** These two-day workshops will focus on how to write good data processing user-manuals with emphasis on analysis of specific user needs, planning and outlining, effective writing, illustration and packaging of documentation. The program includes lectures on basic concepts followed by small group discussions.

Contact Progressive Communications Inc, The Alamo 310, 128 S Tejon St, Colorado Springs CO 80903.

December 10-11

Mini and Microcomputers in Control, Galt Ocean Mile Hotel, Ft Lauderdale FL. This symposium will cover computer architecture and hardware for control, languages for control, algorithms for control, hierarchical control, methodology, and other topics. Contact The Secretary, Computers in Control Symposium, POB 2481, Anaheim CA 92804.

December 10-12

Project Management for Computer Systems, Chicago IL. This seminar will illustrate techniques for planning, implementing, installing, and controlling projects. Contact The University of Chicago, 1307 E 60th St, Chicago IL 60637.

December 10-13

1979 Fall DECUS US Mini/Midi Symposium, San Diego CA. This symposium is an opportunity for Digital Equipment computer users to participate in a technical exchange. Contact DECUS, One Iron Way, MR2-3, Marlboro MA 01752.

December 10-14

IEEE Computer Society's Tutorial Week 79, Hotel Del Coronado, San Diego CA. Fifteen different one-day seminars will be offered throughout the week. Contact IEEE Computer Society, POB 639, Silver Spring MD 20901.

December 10-14

Advanced Programming Workshop, Lafayette IN. Course objectives include developing skills required to plan, prepare, test, and document software. Projects will include using assemblers and high-level language compilers and interpreters. Contact Wintek Corp, 902 N 9th St, Lafayette IN 47904.

JANUARY 1980

January 3-4

Hawaii International Conference on System Sciences, Honolulu HI. The conference will cover developments in theory or practice in software and hardware, and advanced computer systems applications in selected areas with emphasis on medical information processing and computer-based decision support systems for upper level managers in organizations. For more information, contact Perry G Patteson, Office of Management Programs, University of Hawaii, 2404 Maile Way, Honolulu HI 96822.

January 5-8

International Winter Consumer Electronics Show, Las Vegas Convention Center, Grand Ballroom of the Las Vegas Hilton and the Jockey Club Hotel, Las Vegas NV. The show will have over 850 exhibitors covering markets including audio systems, software, television and video tape and disk systems, home computers, calculators, and many more. Contact Consumer Electronics Shows, 2 Illinois Ctr, Suite 1607, 233 N Michigan, Chicago IL 60601.

January 15

Invitational Computer Conference, Orange County CA. New developments in computer and peripheral technology such as Pascal systems, 2-page printers, and streaming tape drives, will be featured in this conference directed to the quantity buyer. For more information, contact B J Johnson and Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach CA 92660.

January 15-18

TV-Microelectronics and Microprocessing Exhibition, National Exhibition Centre, Birmingham, England. Manufacturers and suppliers of microprocessors, electronic and microcomputer games, video display units, video cameras and projection systems, and digital consumer electronics are invited to participate. Over 9000 retailers, wholesalers, distributors and government buying authorities are expected to attend this show. For more information, contact TMAC, 680 Beach, Suite 428, San Francisco CA 94109.

January 23-26

International Microcomputers Minicomputers Microprocessors (IMMM), Harumi Exhibition Centre, Tokyo Japan. This is a show for manufacturers, commercial and financial establishments, service industries and institutions, and design engineers interested in buying computer systems, components and services. For more information, contact Industrial and Scientific Conference Management Inc, 222 W Adams St, Chicago IL 60606.

January 28-30

Communication Networks '80, Sheraton Washington Hotel, Washington DC. The program will offer 50 conference sessions in areas such as fiber optics, satellite communications, systems networks, and innovations in electronic mail and office administrative networks.

For further information on registration, speaking opportunities or exhibit space, contact William Leitch, The Conference Co, 60 Austin St, Newton MA 02160.

January 28-30

Principles of Programming Languages, Las Vegas NV. This symposium concerns practical and theoretical aspects of principles and innovations in the design, definition, and implementation of programming languages. Some topics are algorithms and complexity bounds for language processing tasks, specification languages, error detection and recovery, and unusual or special-purpose languages that raise issues of principle. Contact Professor John Werth, Department of Mathematical Sciences, University of Nevada, Las Vegas NV 89154.

January 30-February 1

MIMI '80 Asilomar, Asilomar Conference Grounds, Pacific Grove CA. This symposium covers all aspects of mini and microcomputers including technology, hardware, software engineering, languages, education and more. Contact The Secretary, MIMI '80 Asilomar, POB 2481, Anaheim CA 92804.

FEBRUARY 1980

February 6

Invitational Computer Conference, Ft Lauderdale FL. This conference is directed to the quantity buyer and will feature the newest developments in computer and peripheral technology. Contact B J Johnson and Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach CA 92660.

February 13-15

The IEEE International Solid State Circuits Conference, San Francisco CA. This conference is a forum for the presentation of advancements in all aspects of solid state circuits. It will cover design, performance, fabrication, testing, and applications in digital, analog, microwave, and other areas of new solid state circuits, device structures, phenomena and systems. For more information, contact Lewis Winner, 301 Almeria Ave, POB 343788, Coral Gables FL 33134.

February 18-21

European Information Management Exhibition and Conference, Wembley Conference Centre, London, England. This show will exhibit microcomputer systems and peripheral items with demonstrations and applications focused on problem solving for the management executive. Contact, Exposonsul, 420 Lexington Ave, New York NY 10017.

February 25-27

Communication Networks '80, Shoreham Americana Hotel, Washinton DC. This conference and exposition will cover business communications. For program information, contact the Director of Program Developement, The Conference Co, 60 Austin St, Newton MA 02160. For exhibit information, contact the national sales manager, Communications Networks '80, POB 96, Haddon Heights NJ 08035.

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Twenty-four Ways to Write a Loop

Dr Maurer Takes You Through a Loop

W D Maurer
Professor Dept of Electrical
Engineering and Computer Science
George Washington University
Washington DC 20052

To start with, let us look at table 1. There are several things about this table that should be surprising.

All we are trying to do is move some quantities from one place to another. There are N of them, and they are called P(1) thru P(N). We are trying to move them to Q(1) thru Q(N), which we could do, of course, using a FOR statement in BASIC, as follows:

```
10 FOR J=1 TO N
20 Q(J)=P(J)
30 NEXT J
```

which should make sense even if you don't know BASIC. But we are trying to do this without a FOR statement, in order to learn how loops function; and immediately we are confronted with a wide variety of choices. Table 1 shows the first twenty-four of these. They are all different; they are all short; and they all do exactly the same thing. (Well, not quite exactly. At the end of some of them, J is equal to N+1; at the ends of others, J may be equal to N, or to 1, or to 0. But since we are presumably not going to use J after we finish the loop, this should make no difference.)

Why are there so many ways to write a loop? There are certain things

Actually, 124 ways (or more) illustrate the endless variety of looping — that simplest of programming techniques

we can do in either of two (or more) ways.

We can start with Q(1) and go up to Q(N) (first and second columns in table 1), or we can start with Q(N) and go down to Q(1) (third and fourth columns).

We have three things to do in the loop: setting Q(J) equal to P(J); increasing (or decreasing) J by one; and making a test. These three things may be arranged in any of six ways; denoting them by U, V, and W, we may arrange them as UVW, UWV, VUW, VWU, WUV, or WVU. Each of these six arrangements corresponds to one of the six rows of table 1.

What may be further surprising about table 1 are the subtle ways in which not everything is quite symmetrical. For example, in the last column, the variable J is sometimes initialized to N, and sometimes to N+1. The latter takes a bit more time (unless N is really a constant, such as 10). In the first column, J is sometimes set to 1 and sometimes to 0, which on many computers takes a bit less time than setting it to 1.

It does not take much ingenuity, however, to see that in enumerating twenty-four ways to write a loop, we have really only scratched the surface. What are some of the other things we could have done?

Looking at the top of the second column, we see that we are testing whether J is less than or equal to N. We could just as easily have tested whether J is less than N+1. The same sort of change could have been made throughout the second and fourth columns, giving us a total of thirty-six ways to write a loop.

Most of the changes of this kind would rather obviously have been changes for the worse. It clearly takes more time testing against N+1 than it does testing against N, even if we set some new variable like N1 to N+1 before the loop and then test against N1 inside the loop. A possible exception to this is the one at the top of the last column, where we could have tested for J greater than 0. In assembly language on a 6800-based system using 8-bit signed integer data, you can do this with a branch-if-greater-than-zero (BGT) instruction directly after the decrementing.

10 J=1 20 Q(J)=P(J) 30 J=J+1 40 IF J<>N+1 GOTO 20	10 J=1 20 Q(J)=P(J) 30 J=J+1 40 IF J<=N GOTO 20	10 J=N 20 Q(J)=P(J) 30 J=J−1 40 IF J<>0 GOTO 20	10 J=N 20 Q(J)=P(J) 30 J=J−1 40 IF J>=1 GOTO 20
10 J=1 20 Q(J)=P(J) 30 IF J=N GOTO 60 40 J=J+1 50 GOTO 20	10 J=1 20 Q(J)=P(J) 30 IF J>=N GOTO 60 40 J=J+1 50 GOTO 20	10 J=N 20 Q(J)=P(J) 30 IF J=1 GOTO 60 40 J=J−1 50 GOTO 20	10 J=N 20 Q(J)=P(J) 30 IF J<=1 GOTO 60 40 J=J−1 50 GOTO 20
10 J=0 20 J=J+1 30 Q(J)=P(J) 40 IF J<>N GOTO 20	10 J=0 20 J=J+1 30 Q(J)=P(J) 40 IF J<N GOTO 20	10 J=N+1 20 J=J−1 30 Q(J)=P(J) 40 IF J<>1 GOTO 20	10 J=N+1 20 J=J−1 30 Q(J)=P(J) 40 IF J>1 GOTO 20
10 J=0 20 J=J+1 30 IF J=N+1 GOTO 60 40 Q(J)=P(J) 50 GOTO 20	10 J=0 20 J=J+1 30 IF J>N GOTO 60 40 Q(J)=P(J) 50 GOTO 20	10 J=N+1 20 J=J−1 30 IF J=0 GOTO 60 40 Q(J)=P(J) 50 GOTO 20	10 J=N+1 20 J=J−1 30 IF J<=0 GOTO 60 40 Q(J)=P(J) 50 GOTO 20
10 J=1 20 IF J=N+1 GOTO 60 30 Q(J)=P(J) 40 J=J+1 50 GOTO 20	10 J=1 20 IF J>N GOTO 60 30 Q(J)=P(J) 40 J=J+1 50 GOTO 20	10 J=N 20 IF J=0 GOTO 60 30 Q(J)=P(J) 40 J=J−1 50 GOTO 20	10 J=N 20 IF J<=0 GOTO 60 30 Q(J)=P(J) 40 J=J−1 50 GOTO 20
10 J=0 20 IF J=N GOTO 60 30 J=J+1 40 Q(J)=P(J) 50 GOTO 20	10 J=0 20 IF J>=N GOTO 60 30 J=J+1 40 Q(J)=P(J) 50 GOTO 20	10 J=N+1 20 IF J=1 GOTO 60 30 J=J−1 40 Q(J)=P(J) 50 GOTO 20	10 J=N+1 20 IF J<=1 GOTO 60 30 J=J−1 40 Q(J)=P(J) 50 GOTO 20

Table 1: *Twenty-four ways to write a loop in BASIC. These twenty-four basic methods can be expanded with a variety of small changes to produce over 124 different types of looping.*

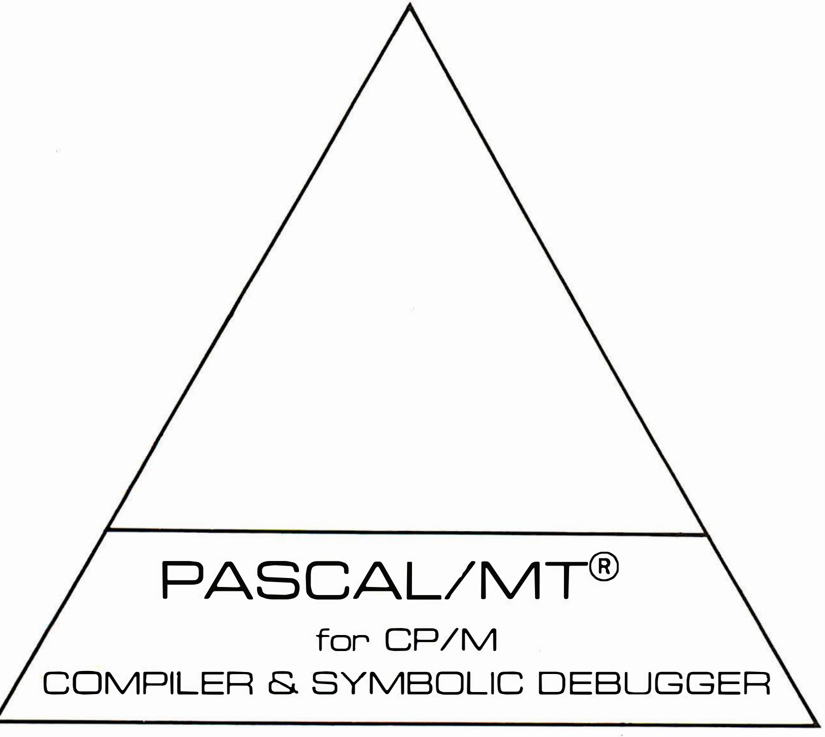
We can consider the possibility of setting Q(J+1) to P(J+1), or Q(J−1) to P(J−1), rather than Q(J) to P(J). In some cases, this would speed up some of the other operations in the loop. For example, at the top of the first column, we could have set J to 0 and tested J against N rather than N+1, if we set Q(J+1) equal to P(J+1). Both of these changes represent timing improvements.

It might seem that setting Q(J+1) to P(J+1) wastes a certain amount of time of its own, compared with setting Q(J) equal to P(J). This, however, is not so, or should not be so on a well-constructed system (although it might be so in some versions of BASIC). Any additive or subtractive constant in a subscript (such as J+1, above) does not have to be computed. To see why this is so, we need some knowledge of assembly language; those who know only BASIC may skip the following paragraph, in which the explanation is given.

Every time we make reference to $t(v)$, for an array t and a variable v, we have to add the value of v to the address of t. On the 8080, this is done explicitly; we typically do an LXI H,t followed by a DAD D where the DE register contains v (that is, where the E register contains v and the D register contains 0) and then we can reference $t(v)$ by doing ADD M or MOV r,M or MOV M,r or the like. On the 6502, it is done in the hardware; we do an LDA t,X or an STA t,X or an ADC t,X or the like, where the X register contains v, but the hardware adds the X register to the address given in the instruction, which effectively adds v to the address of t in this case. Every microcomputer has slightly different details, but the idea is the same in all cases. Now suppose we want to make a reference to $t(v+k)$, where k is a constant. We have to add the value of $v+k$ to the address of t — which is the same as adding the value of v to the address of t plus k. The point is that both k and the address of t are constants; they do not change during the running of this program. Thus the address of t plus k is also a constant, and this addition can be done before the program starts. On the 8080, for instance, we would simply say LXI H,$t+k$ rather than LXI H,t; this is a single instruction whose address field (second and third bytes of the instruction code) contains the 16-bit quantity obtained by adding k to the address of t. On the 6502, we might say LDA $t+k$,X and again we have a single instruction whose address field contains the address of t plus k. The same trick works, of course, for references to $t(v-k)$ rather than $t(v+k)$.

At any rate, by adding 1 or subtracting 1 in our subscripts, we have produced two new ways of writing a loop from every way we already have. We now have 108 ways to write a loop. Of course, theoretically, we could have set Q(J+2) equal to P(J+2), or Q(J−2) equal to P(J−2),

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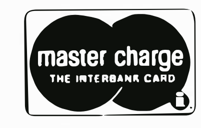
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and so on ad infinitum. There is now no bound at all (except for integer overflow considerations) on the number of new ways to write a loop we can set down.

One of these, by the way, has a certain amount of practical importance. The IM6100 microcomputer (or PDP-8) has an increment instruction, but no decrement instructions. Furthermore, the increment does a test against 0 (it is called ISZ, or increment and skip on 0). This does not correspond to anything in table 1 at all; if we are testing against 0, in table 1, we are always decrementing. However, consider the following loop:

```
10 J=-N
20 Q(J+N+1)=P(J+N+1)
30 J=J+1
40 IF J < > 0 GOTO 20
```

This time we cannot use the trick we mentioned earlier unless N is a constant. If N is a constant, however, the above loop does the same thing as all the other loops of table 1; and the last two instructions in it are meant to be executed, on the IM6100, by the single instruction ISZ J, followed by a jump to the label 20.

Are we finished with all possible speed improvements in our loop? Not at all. Consider the following loop:

```
10 J=2
20 Q(J-1)=P(J-1)
30 Q(J)=P(J)
40 J=J+2
50 IF J< =N GOTO 20
```

Suppose that N is 100. Then, instead of going through this loop one hundred times, we would go through it fifty times. Each time, *two* elements of the Q array would be set to corresponding elements in the P array. The advantage is that J=J+2 is done only fifty times, where J=J+1 was done one hundred times in the loops of table 1; also, the IF statement is done only fifty times instead of one hundred times.

In practice, the improvement here is not quite as good as it looks. The assignment J=J+2 is generally slower than J=J+1. In fact, on many microcomputers, the fastest way to do J=J+2 is to do J=J+1 twice. On the 6502, the two array assignments can be done very neatly, one after the other, with:

```
LDA P-1,X
STA Q-1,X
LDA P,X
STA Q,X
```

as soon as the value of J is in the X register. On the 8080, though, assuming that the address of P(J−1) is in DE and the address of Q(J−1) is in HL, you would have to do something like:

```
LDAX D
MOV M,A
INX D
INX H
LDAX D
MOV M,A
INX D
INX H
```

where the second INX D and INX H set up the DE and HL registers for the next time through the loop. Thus the only improvement here is in having fewer executions of the test at the end of the loop.

Obviously the same idea as above could be implemented by increasing the variable J by 3, by 4, or however many each time, although there will be a corresponding increase in the size of program memory. Another difficulty with these schemes is that they do not work unless J is a multiple of 2, or whatever the increment is. If this is not the case, then some extra elements will be transferred from one array to the other, and this may cause unpredictable results. The general technique (known as "unrolling" a loop) does, however, have some useful applications on big computers. Even on a small system it is often useful, particularly when N is a very small number, such as 3, to write:

```
10 Q(1)=P(1)
20 Q(2)=P(2)
30 Q(3)=P(3)
```

which is better than any of the loops we have so far discussed.

Another speed improvement in loops arises from an analysis of the case in which N=0. If we are moving N quantities, then, if N is 0, we should be moving no quantities; that is, we should be doing nothing at all. Many of our loops, however, either become endless, or they move a single quantity (P(1) or P(N)) in this case. In particular, this holds for all of the loops in the first and third rows of table 1. The reason that this is a bit unsettling is that these are the only loops in table 1 which have three repeated statements in them (line numbers 20, 30, and 40). They are therefore the fastest of our loops, since all the other loops in table 1 have four repeated statements (line numbers 20, 30, 40, and 50).

It would seem that we have a choice between slowing down our loops and having a loop that doesn't work for N=0. In FORTRAN, in fact, the choice that was made was to disregard the case N=0 in favor of a faster loop. (This could be called an "institutionalized bug" in FORTRAN.) After all, the FORTRAN people reasoned, we can always check if N=0 just before starting the loop, if we are worried about this case. But there is a better way; we can write:

```
10 J=1
20 GOTO 50
30 Q(J)=P(J)
40 J=J+1
50 IF J < =N GOTO 30
```

thus having only three repeated statements (line numbers 30, 40, and 50) and a loop which works properly if N=0.

It might seem as if the above loop is violating a sacred precept by jumping into the middle of the loop (at line number 20). In fact, however, the problems associated with jumping into the middle of a loop do not apply to the special case of jumping to one of the incrementation and testing statements at the end of the loop, provided that we know what we are doing. (If we have a FOR loop in BASIC, we still can't jump from outside the loop to the NEXT statement at the end of it; we are merely talking about ways in which the FOR loop might be implemented.)

Let us now take up the general subject of implementation of loops in machine language.

In the first place, there are a few computers that perform certain loops in hardware. That is, there is a single instruction that performs an entire loop. On the Z80, the instructions LDIR, LDDR, CPIR, CPDR, INIR, INDR, OUTIR, and OUTDR are of this type. Single instructions that perform loops are also found on certain

big computers; thus the UNIVAC 1106 and other computers of the 1100 series have block transfer, search, and masked search instructions, and the now obsolete UNIVAC 1103 had a special instruction called "repeat" that caused the instruction which followed it to be repeated a specified number of times. The trouble with such instructions is that each of them is an implementation of only one specific type of loop, although an admittedly common one. For example, on the Z80, as long as the value of N is in the double register BC, we can perform the data-moving operation of table 1 by either of the sequences:

```
LD  DE,Q
LD  HL,P
LDIR
```

or:

```
LD  DE,QEND
LD  HL,PEND
LDDR
```

assuming that the arrays P and Q end at PEND and QEND respectively. (These two sequences correspond roughly to the second and fourth columns of table 1, respectively.) While this gives a significant speed improvement in this case, it is of no help if the repeated instruction, instead of Q(J)=P(J), is Q(J)=J or Q(J)=0 or R(J)=P(J)+Q(J), or if the count could have been kept in the B register while the C register is used to hold something else. The same sort of thing could also be done in one instruction on the UNIVAC 1106, using a block transfer instruction.

In the second place, even if an entire loop cannot be executed by means of a single instruction, some microcomputers have a single instruction which performs the functions associated with the loop index — that is, increasing it or decreasing it by 1 and then performing a conditional transfer. On the Z80, there is DJNZ, which decrements the B register by one and jumps (presumably back to the start of the loop) unless the B register has been decreased to 0. On the Signetics 2650, there is BDRR, which does the same thing with any specified register; there is also BDRA, which performs a jump to an absolute rather than a relative address, and BIRR and BIRA, which increment instead of decrementing. The EA9002's DRJ and IRJ are also similar. The 8080, the 6800, the 6502, and the COSMAC, however, have no instructions of this kind, although it is a technique very common on big computers.

Even though there may not be a single instruction on your processor that decreases a register by 1 and also does a conditional jump, this method of ending a loop is the one that is the most common on small systems. It corresponds to the loop at the top of the third column in table 1. Typically, you use the B register on the 8080 and 6800 and the Y register on the 6502. The decrementing instruction (DCRB on the 8080, DECB on the 6800, DEY on the 6502) sets the zero flag, so that a jump on nonzero (JNZ on the 8080 and BNE on the 6800 and 6502) can immediately follow. On the COSMAC, there is no zero flag; after decrementing, the register that was decremented must be moved to the D register before the branch on nonzero (BNZ).

One important difference between the typical loop and the one at the top of the third column in table 1 is that the movement of data in that loop proceeds backwards; that is, Q(N) first, then Q(N−1), and so on. In many loops the logic makes this impossible, and in any event it is unnecessary. Even if we have a register which decrements to 0 during a loop, we usually have one or more further indices which are initialized at the beginning of the loop and which increase, rather than decreasing, every time we start a new iteration.

Figure 1 illustrates the progress of such a loop. The loop moves the string DATA from one place to another in memory; it is given for the 8080 by:

```
LOOP: LDAX D
      MOV M,A
      INX D
      INX H
      DCR B
      JNZ LOOP
```

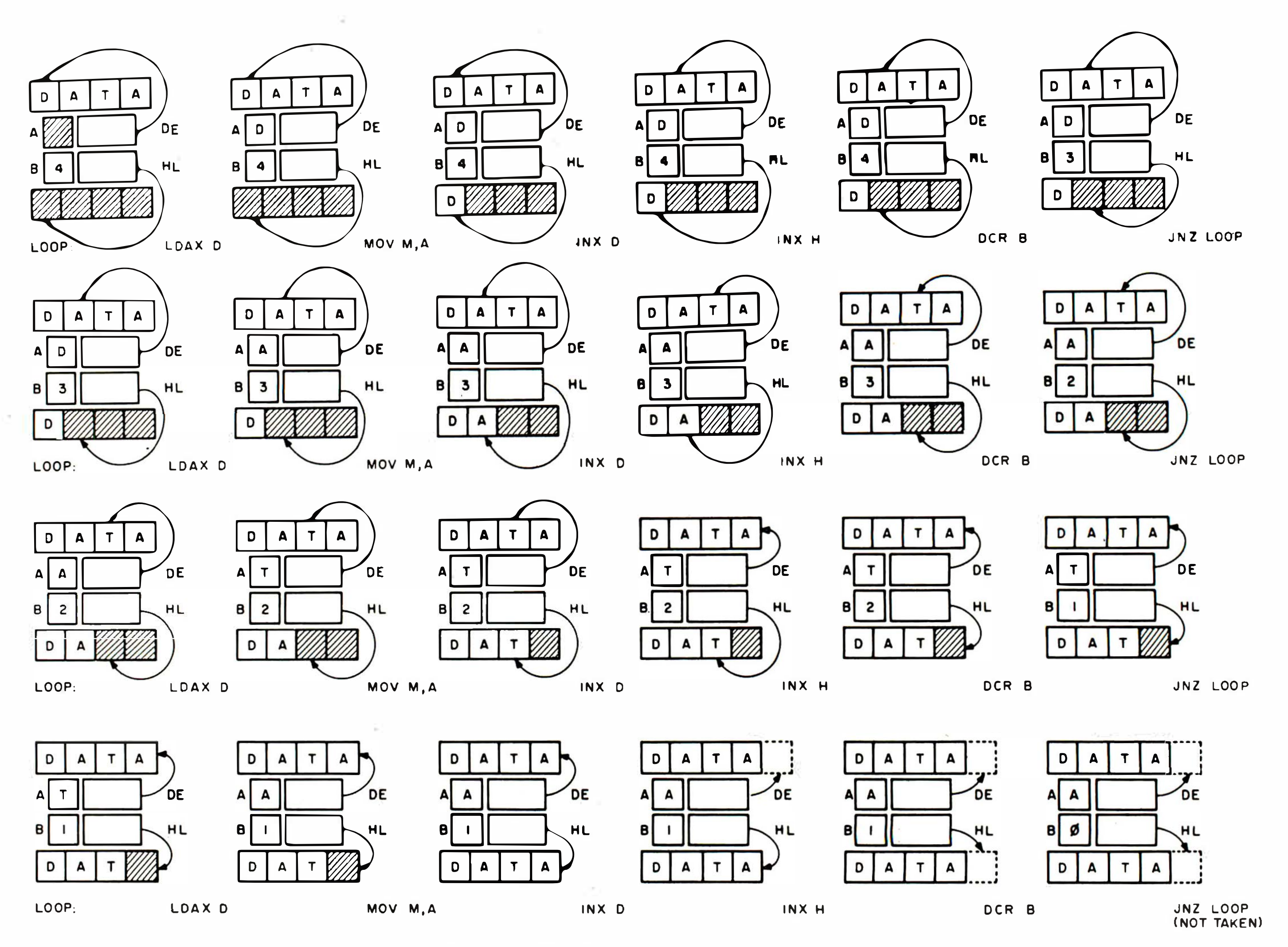


Figure 1: *Progress through a loop to move the string "DATA" from one place in memory to another.*

where the registers B, DE, and HL are presumed to be loaded before the loop starts. Specifically, register B is loaded with the number of characters to be moved (four, in this case); DE is loaded with the *source starting address*, or the address of the first character of the string in its old location; and HL is loaded with the *destination starting address*, or the address of the first character of the string in its new location. The six instructions of the loop are executed four times each, and the contents of the A, B, DE, and HL registers and the source and destination string area are illustrated. In the case of the DE and HL registers, an arrow is drawn from the register to the cell with address α, where the number α is currently in the given register. (We say that the register contains a *pointer* to that cell, or *points* to that cell.) The six instructions take 7, 7, 5, 5, 5, and 10 cycles respectively, giving a total timing of $39n$ cycles for n characters to be moved; in this case it would be 156 cycles, or 78 µs if a 500 ns clock is used. To this must be added, of course, the time taken for initialization; using LXI D, α and LXI H, β and MVI B,4, the total time would become 93µs in this case.

If you are new at writing assembly language code, do not worry if it takes you a while to get used to loops. Endless loops, and loops which are supposed to be done n times but which in fact are done either $n+1$ times or $n-1$ times, are quite commonly written by beginning programmers. The most important rules to remember are the following:

- When you jump back to the start of the loop, *never* jump back to the place where you set up the count or the starting addresses (registers B, DE, and HL in the example above). This will *always* result in an endless loop. You should jump back to the point immediately following this initialization, as it is called.
- Remember that sometimes a loop must start with the count set to N, sometimes to N+1, and sometimes to N−1, depending on the logic. You should "walk through" your loops a few times when you are just starting out, until you are sure of the proper starting values.
- If you are using a step size greater than one, try not to test for equal or unequal. For example, if you are looping for J=1 to 10 by steps of two (FOR J=1 TO 10 STEP 2 in BASIC) then the values of J will be 1, 3, 5, 7, 9, 11, and so on; if your test at the end of the loop is a test for J=10, then J=10 will never hold and the loop will become endless. A test involving > or < (such as J<=10) will avoid this difficulty. ■

Morse Code Trainer

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A commonly suggested application for microprocessors is translating text to Morse code. The subroutine described in figure 1 translates letters into Morse code and drives a speaker to serve as a Morse code trainer. Minor changes to the speaker driver routine would enable a microcomputer to key a transmitter directly.

The main entry to the routine is at hexadecimal address 0180. When the routine is called, the letter to be transmitted must be stored in register A as a number between decimal 0 and 25: 0=A, 1=B and 25=Z. By subtracting hexadecimal 41 from an ASCII letter code, this routine may be made compatible with ASCII text handling programs.

The program in listing 1 is relocatable. A data table (table 1) is expected to start at hexadecimal location 0080. The table may be relocated by changing the address stored in hexadecimal memory locations 0181 and 0182 to point at the location before the first word of the table.

Since the translation routine alters the contents of all registers, the user must write the mainline logic defensively. Registers containing important information must be saved by the user before calling the Morse code translator.

Intermediate Code

The heart of the Morse code translator is a binary representation of Morse code, illustrated in figure 2. This representation is stored in a data table for each letter, starting at hexadecimal 0080. The first letter's code is stored in the first position, the second letter's code in the next position, and so forth through the alphabet.

The intermediate code (stored as a binary coded decimal number) is very simple. The four high order bits define the number of dots or dashes in the letter. The four low order bits determine the sequence of dots and dashes for the letter. The first dot or dash is stored in the low order bit, with a 1 indicating a dash and a 0 indicating a dot.

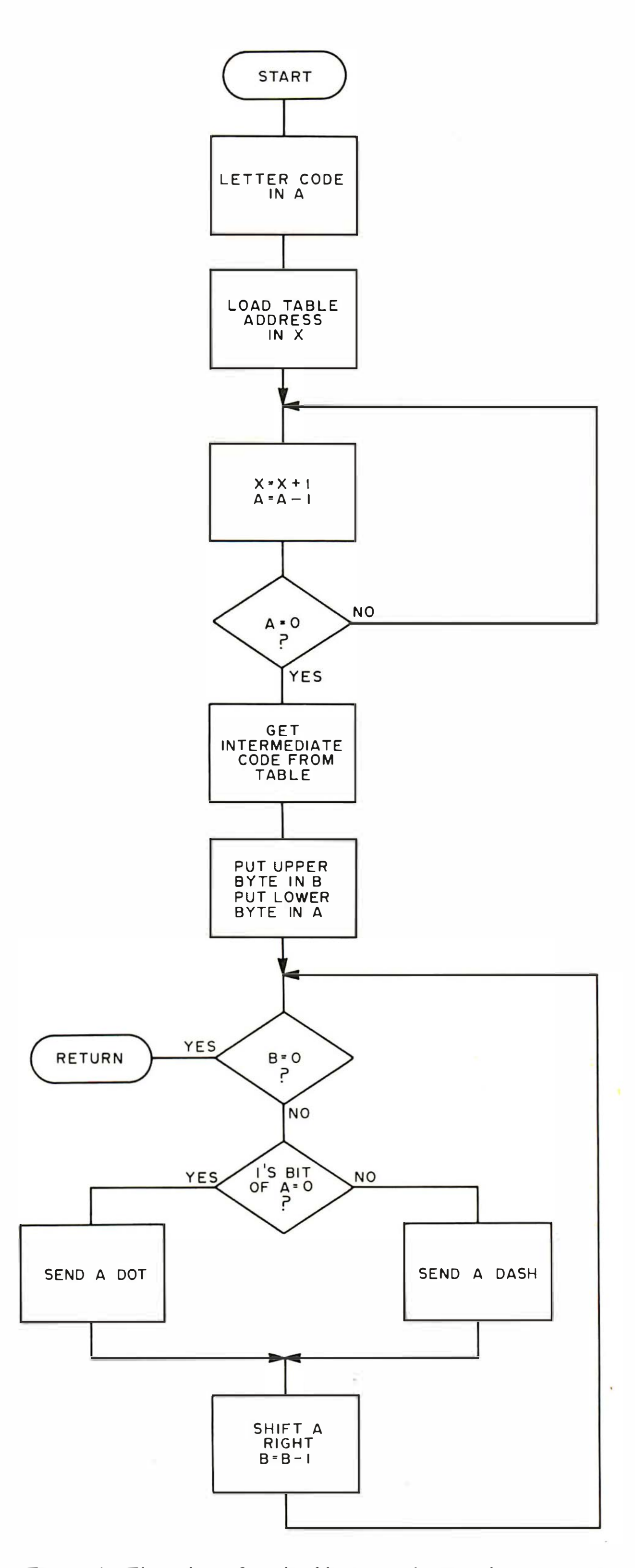


Figure 1: Flowchart for the Morse code translation routine.

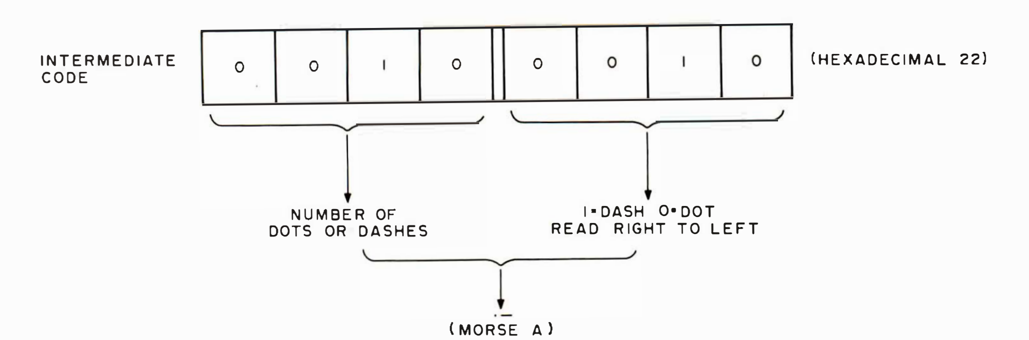


Figure 2: Intermediate code used by the ASCII-to-Morse-code translator. The data is stored in binary coded decimal (BCD) format. The high order bit indicates how many characters are in the letter; the low order bit defines whether they are dashes or dots.

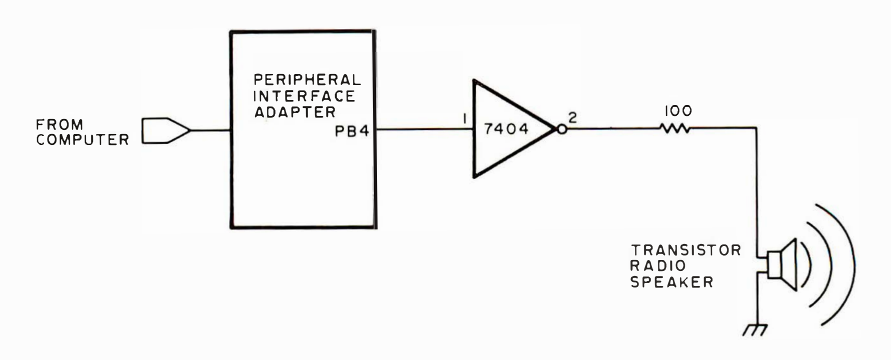


Figure 3: Simple circuit for connecting a speaker to the computer output port for listening to computer output in Morse code.

Hexadecimal Address	Hexadecimal Code			Mnemonic Op Code	Operand	Comments
0178	16			TAB		entry for byte splitter
0179	84	OF		AND		get low byte
017B	54	54		LSR	LSR	shift right four times
017D	54	54		LSR	LSR	to get high order byte
017F	39			RTS		
0180	CE	00	7F	LDX		main entry: point X to byte before start of data table
0183	08			INX		
0184	4A			DEC	A	point X to Ath entry
0185	2A	FC		BPL		
0187	A6	00		LDA	A	fetch intermediate code
0189	8D	ED		BSR		call byte splitter (0178)
018B	5D			TST	B	all signals sent?
018C	26	01		BNE		
018E	39			RTS		all done
018F	85	01		BIT	A	check lowest bit of A
0191	27	04		BEQ		jump if zero (dot)
0193	8D	08		BSR		send a dash
0195	20	02		BRA		skip
0197	8D	17		BSR		send a dot
0199	44			LSR	A	shift A to get next signal code
019A	5A			DEC	B	
019B	20	EE		BRA		start another pass through loop
019D	CE	20	00	LDX		load timer for a dash
01A0	OF			SEI		start tone here
01A1	09			DEX		
01A2	27	05		BEQ		all done?
01A4	7C	80	06	INC		increment PIA
01A7	20	F8		BRA		start a new loop
01A9	CE	10	00	LDX		start a pause after tone
01AC	09			DEX		loop for a while
01AD	26	FD		BNE		
01AF	39			RTS		tone finished
01B0	CE	10	00	LDX		load timer for a dot
01B3	8D	EB		BSR		go to tone generator
01B5	39			RTS		

Listing 1: Morse code conversion program written in 6800 assembler code. This program can be relocated without any change.

The 2's bit gives the second dot or dash, if necessary, and so forth. For example, the code for A (— ·) is hexadecimal 22 (0010 0010).

How it Works

The subroutine in listing 1 loads the index register with the starting address of the intermediate code table. The code indicated by register A is fetched, and the four high order bits are split off by a call to the subroutine at hexadecimal 0178 and stored in register B.

The low order bit of register A, which contains the code for a dot or dash, is now tested. If a dash is to be sent, the dash generator routine is called (hexadecimal 019B). A dot is handled by the dot generator routine (hexadecimal 01B0). These routines drive a speaker. They may be rewritten to drive a transmitter interface.

The speaker driving routines begin by setting a timing value into the index register. The values given in listing 1 (dot=1000, dash=2000) result in sending speeds of about seven words per minute on my computer using a 614 kHz clock speed. Different speeds and dot-to-dash ratios may be obtained by changing these values.

The speaker is actually driven by the instruction sequence beginning at hexadecimal 01A0. This loop subtracts 1 from the index register and adds 1 to an output port. The use of a peripheral interface adapter (PIA) is assumed by this program. The address of the output port is stored in hexadecimal locations 01A5 and 01A6 until the X register is 0. The initial value of the X register determines the length of the tone. The program assumes that the appropriate output port has been initialized. By adding 1 to the output port each time the routine loops, the low order bit (PB0) changes very rapidly, the second bit (PB1) only half as quickly, and so forth; each bit gives a different tone. The speaker is connected to one output bit via a buffer, which provides sufficient drive capacity to power the speaker arrangement in figure 3. Users may select any bit to fit their own tonal preference.

After each dot or dash is sent, the main subroutine performs a logical shift right on register A. This places the next dot or dash code into the low order bit. Register B is decremented, and the program tests whether it is 0. If so, the entire letter has been sent. If register B is not 0, the program loops until all dots and dashes have been sent. Control is then returned to the user's mainline program.■

Hexadecimal Address	Hex Code	Letter	Morse
0080	22	A	·—
0081	41	B	—···
0082	45	C	—·—·
0083	31	D	—··
0084	10	E	·
0085	44	F	··—·
0086	33	G	——·
0087	40	H	····
0088	20	I	··
0089	4E	J	·———
008A	35	K	—·—
008B	42	L	·—··
008C	23	M	——
008D	21	N	—·
008E	37	O	———
008F	46	P	·——·
0090	4B	Q	——·—
0091	32	R	·—·
0092	30	S	···
0093	11	T	—
0094	34	U	··—
0095	48	V	···—
0096	36	W	·——
0097	49	X	—··—
0098	4D	Y	—·——
0099	43	Z	——··

Table 1: Intermediate code data table is expected by the program to start at hexadecimal memory location 0080.

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For more information, contact Texas Instruments, POB 1444, M/S 7784, Houston TX 77001.

Coming up in BYTE

In the January 1980 issue of BYTE, the theme is "The Domesticated Computer" — the idea of using computers around the home in various forms. A key part of that theme is played by Steve Ciarcia's article (written with some research aid from Ira Rampil) on adapting a widely sold and mass-produced household electrical controller to the typical personal computer.

Thirty Days to a Faster Input

Arthur Armstrong
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Los Angeles CA 90066

Remember the last time you typed something into your computer? Did you look at the text to find out what to type, then at the keyboard to find out how to type it, then at the screen to see what you had typed? If you did, then it's time you learned to touch type. This is simply a means of learning the positions of the keys so well that typing becomes unconscious and automatic, and the material seems to flow directly from your mind to the page. The mechanical process becomes completely removed from the cerebral process, much like a musician playing an instrument.

Learning touch typing is not difficult. (Consider the millions of people who have mastered it.) All it takes is a convenient and permanent assignment of fingers to keys, some way of measuring progress, and a lot of systematic practice. Fortunately for you, your computer can perform all the tedious error checking and bookkeeping while you concentrate on the process. The program listed at the end of this article will help you become, if not rich and famous, at least less frustrated in your typing.

Admittedly, the traditional keyboard is not an efficient one. However, if that is what you have, you should use the conventional finger assignment shown in figure 1. Naturally, the keys work no matter what finger you use, but this scheme seems comfortable. The important thing is to always use the same finger for each key. Otherwise the process cannot become automatic.

The program will ask you what characters you want to practice. This allows you to learn groups rather than to attempt the entire keyboard at once. One good way is to start with the group ASDFG. When you have mastered these learn HJKL;. Then combine the entire row ASDFGHJKL;. (Use lower case if your keyboard makes this easier. Don't complicate things with the shift key until later.) As you type, keep the tips of the fingers resting on the "home" keys ASDF JKL;. This gives you a fixed reference for reaching other keys. After you have gained facility with the home row, use groups that will allow you to keep a reference on the home keys. Try groups like QWASZX or TYGHBN. This gives you practice in reaching up and down the board. If you try to learn each row separately, you will lose the sense of distance between rows.

The program then asks, "How many in each word?" This means how many of the characters from your group should be presented at one time. When starting a new group of keys, use a word length of one character. When you have learned the individual characters, increase the word length using the same group: this will allow you to develop rhythm. The time interval between keystrokes should always be the same, and don't worry about speed. If you work on accuracy and rhythm, the speed will develop. As you gain facility, use long word lengths (20 to 30) and include spaces in your groups. This gives a sense of typing sets of words.

Figure 1: Standard touch typing finger assignments for the conventional typewriter keyboard.

Stereotyping

The program asks if you want "echo." This means do you want to see the letters you are typing. Perhaps it is better to use echo until you have gained confidence but your goal should be to type with no echo and without looking at the keyboard. If you find yourself peeking at the board use smaller groups of letters. Learn to type while looking only at the text you are copying.

Notes On the Program

Line Numbers	Commentary
100-130	Establishes the values for one set of trials. WL is word length. NT is number of trials. E is echo flag.
200-380	Constitutes the main loop presenting the trials. NP is the number of keystrokes possible.
220	Sets A$ to a null string. 230-260 select a random set of characters and form the word, A$, to be presented.
250	A catenation of strings. MID$ (C$,R,1) selects one character of C$ from position R.
270	Prints the word.
300-370	The input loop.
310	Gets one character from the keyboard (decimal ASCII, no parity).
315	Converts the value to a string.
320	Checks for echo and prints the character if echo is on.
350	Compares the input character with the appropriate character in the test word. If they are not the same, the program jumps to line 500 for error processing. If the character is correct, line 360 tallies the number right (NR) and 370 returns for the next input character.
375	Checks the echo flag and prints a new line if echo is on.
400-430	Presents the results of the trials. 400 calculates the percentage of correct keystrokes based on number right and number possible.
405-410	Tabulates the characters missed.
500-540	Keeps score on wrong characters. The missed character is in A$ pointed to by I. This character is compared with the characters in C$ using J as a pointer. When a match is found, line 515 tallies the miss in array A.
520	Tells you which character you missed.
530	A delay loop to allow time to respond to the error notice.
540	Goes back to the main loop for the next trial.

```
10 REM TYPING DRILL
20 REM ART ARMSTRONG
30 REM 9/8/77
50 CLEAR200
100 INPUT"WHAT CHARACTERS DO YOU WANT";C$
105 L=LEN(C$):DIMA(L)
110 INPUT"HOW MANY IN EACH WORD";WL
120 INPUT"DO YOU WANT ECHO";A$
125 IFLEFT$(A$,1)="Y"THENE=1
130 INPUT"HOW MANY TRIALS";NT
200 FORT=1TONT
210 NP=NP+WL
220 A$=""
230 FORI=1TOWL
240 R=INT(L*RND(1)+1)
250 A$=A$+MID$(C$,R,1)
260 NEXT
270 PRINT:PRINTA$
300 FORI=1TOWL
310 WAIT0,1,1:X=INP(1)AND127
315 B$=CHR$(X)
320 IFE=0THEN350
330 PRINTB$;
350 IFB$<>MID$(A$,I,1)THEN500
360 NR=NR+1
370 NEXT
375 IFE=1THENPRINT
380 NEXTT
400 PRINT:PRINT"YOUR SCORE IS ";INT(100*NR/NP);"%"
402 IFNP=NPTHEN415
405 PRINT"ERRORS:":FORI=1TOL:IFA(I)=0THEN410
407 PRINTMID$(C$,I,1);A(I)
410 NEXT
415 PRINT:INPUT"AGAIN";A$
420 IFLEFT$(A$,1)="Y"THENRUN
430 END
500 FORJ=1TOL
510 IFMID$(C$,J,1)<>MID$(A$,I,1)THEN NEXT:GOTO520
515 A(J)=A(J)+1
520 PRINT:PRINT"ERROR ON ";MID$(A$,I,1)
530 FORI=1TO300:NEXT
540 GOTO380
```

Listing 1: A BASIC program designed to teach touch typing. The user inputs the subset of typing characters to be used in the drill, and the program responds with random combinations of these characters. The user then attempts to duplicate this string of characters by touch typing only (ie: without looking at the keyboard). Any mistakes are immediately signalled by the computer, and the score is printed out. The program was written for MITS 3.2 BASIC and requires 8 K of programmable memory. Any BASIC package that features numeric arrays, strings, and a random number generation capability will suffice.

```
RUN
WHAT CHARACTERS DO YOU WANT? ASDFGHJKL;
HOW MANY IN EACH WORD? 6
DO YOU WANT ECHO? YES
HOW MANY TRIALS? 3

SKFHKS
SD
ERROR ON K

GLFGLF
GLFGLF

GFGDDA
GFGDDS
ERROR ON A

YOUR SCORE IS  66 %
ERRORS:
A 1
K 1

AGAIN? YES
WHAT CHARACTERS DO YOU WANT? ASDFGHJKL;
HOW MANY IN EACH WORD? 6
DO YOU WANT ECHO? NO
HOW MANY TRIALS? 3

AAAS;J

GLSDSF

ERROR ON S

AAFFGF

ERROR ON G

YOUR SCORE IS  77 %
ERRORS:
S 1
G 1

AGAIN? YES
WHAT CHARACTERS DO YOU WANT? SG
HOW MANY IN EACH WORD? 10
DO YOU WANT ECHO? N
HOW MANY TRIALS? 2

SGSSGSSGGS

GGGSGSGSSG

YOUR SCORE IS  100 %

AGAIN? NO
```

Listing 2: A sample touch typing program.

The program then asks, "How many trials?" This is the number of times the program will present you with a word before telling you your score.

After you have finished the set, the program will indicate your score and show you a tabulation of your errors. Note that the program checks each character as it is typed in. It doesn't wait for you to finish the word. As soon as you miss a character, the program tells you which one it was and gives you another word. This is to prevent learning wrong responses.

The program was written in MITS 3.2 8 K BASIC but should be easy to modify for other dialects if necessary.

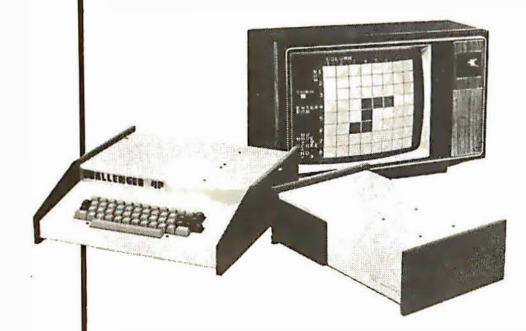
One extension would be to modify the program to select words or phrases from DATA statements. This would allow you to practice on "real" words instead of random strings.

In any event, I hope this turns out to be your type of program!■

What's New?

SYSTEMS

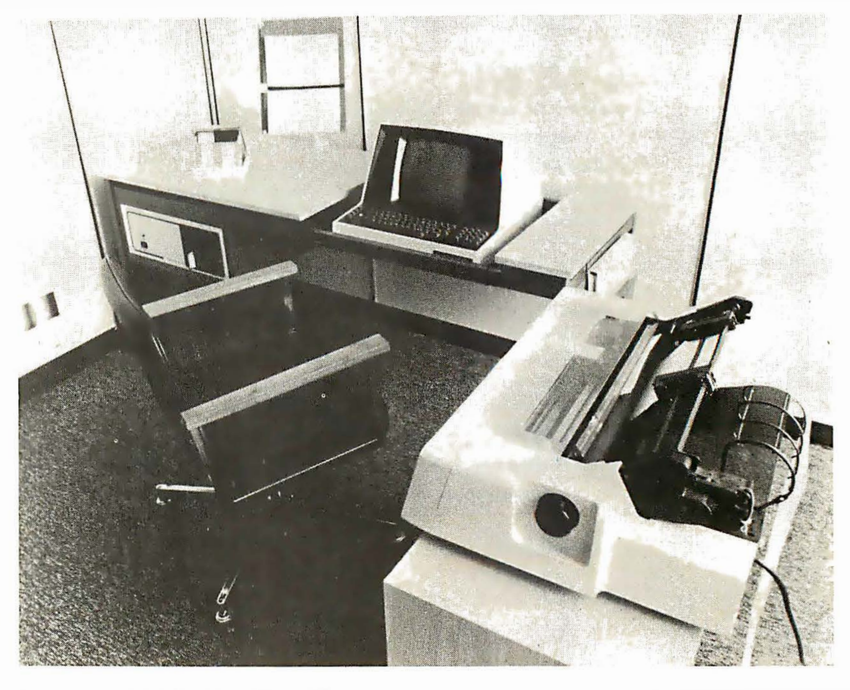
C4P MF Personal Computer



Ohio Scientific has introduced the C4P MF computer which includes a 32 by 64 character display, a 24 K byte static random access memory which is expandable to 48 K bytes and two 5-inch floppy disks. The system features a line printer and modem interface, keyboard with lowercase, and software including a word processor and library of program development tools, high-speed animation, sound output, a digital-to-analog (D/A) converter for music and voice output, joystick interfaces, a home control operating system, an AC remote control interface, and a home security and fire alarm interface.

The price is $1695. For further information, contact Nancy M Valent, Ohio Scientific, 1333 Chillicothe Rd, Aurora OH 44202.

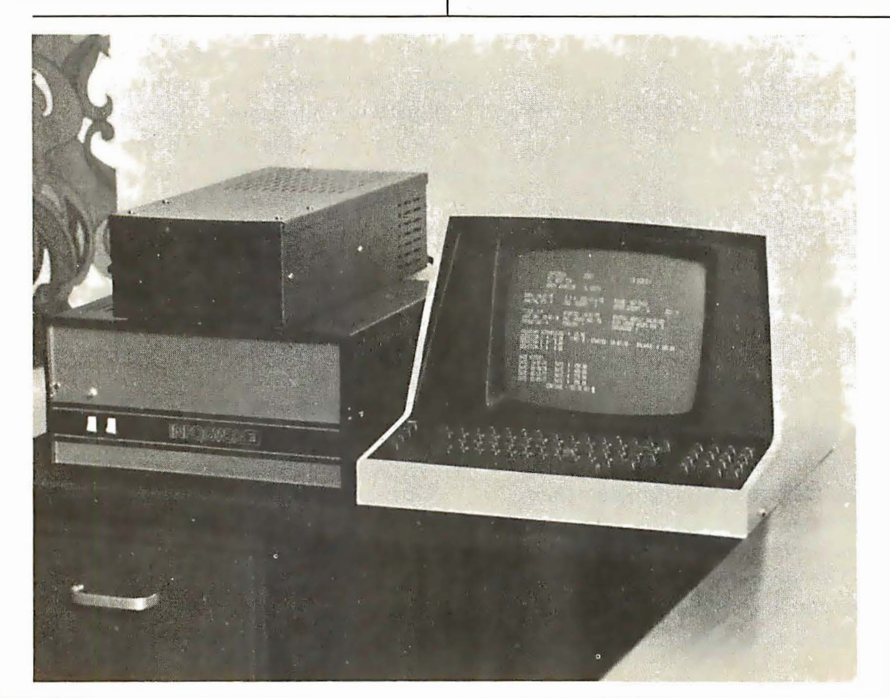
Circle 578 on inquiry card.



System 8000 for Small Business

This microprocessor-based small system incorporates S-100 bus architecture and up to 64 K bytes of programmable memory. Called the System 8000, this product includes a Z80-based processor, a video terminal, a dot matrix printer, and a floppy disk subsystem ranging in storage from 180 K bytes to 2 M bytes. The video terminal has a 12-inch screen displaying 80 characters on each of 24 lines. The printer has a 7 by 7 dot matrix with bidirectional printing capability and rear tractor feed. Software used by the System 8000 consists of the CP/M operating system with an interpreted or compiled BASIC language. Some of the software options include FORTRAN, COBOL and APL. For further information, contact Computer Markets, 75 the Donway W #910, Don Mills, Ontario, CANADA M3C 2E9.

Circle 579 on inquiry card.



Z80 Microprocessor-Based System

Informer 3's hardware consists of a Z80 microprocessor; 48 K bytes of programmable memory; two RS-232 serial interface ports; one parallel interface port; a software monitor in 2 K bytes of programmable read-only memory; 8-inch floppy disk; and a 24-line by 80-character video terminal. The software includes Floppy BASIC (an extended disk BASIC); diagnostics; and basic utilities, which include file copy and disk copy for either single or multiple drive systems. The business software includes inventory management, payroll, accounts payable and receivable, word processing, customer mailing list, general ledger, program development, and others.

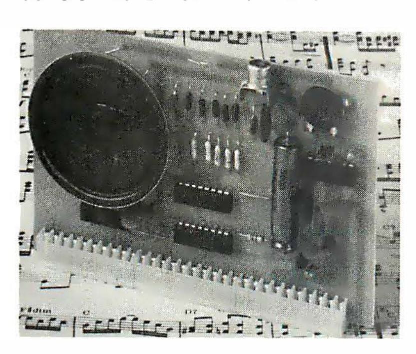
The Informer 3 system sells for less than $4000. For further information, contact Digital Sport Systems, Division of Rohner Machine Works, 7th and Elm, W Liberty IA 52776.

Circle 580 on Inquiry card.

What's New?

PERIPHERALS

Percom Adds Music Board to SS-50 Product Line



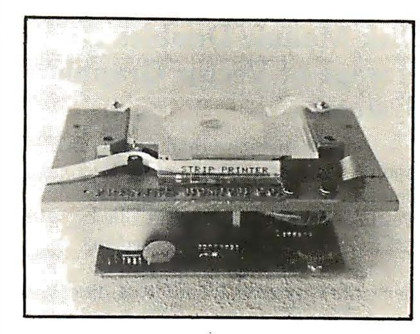
Percom Data Co has added the Newtech Model 68 Music Board to its SS-50 bus product line. The Music Board produces computer generated sounds such as melodies and rhythms, computer game sound effects, Morse code sounds, audible prompts for interactive computer operation, train sounds for model railroading, play-along and sing-along music, and sounds for many other applications.

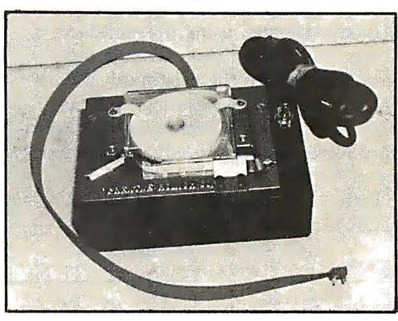
The Music Board uses a single I/O (input/output) slot of Southwest Technical Products' 6800 computer and is supplied with a comprehensive user's manual that includes a theory of operation, a BASIC program for writing music scores, and an assembly language routine for program execution. The card includes address decoding, digital-to-analog conversion, audio amplification circuits, and its own speakers. The audio circuit includes a volume control. An auxiliary jack for connecting the ouput audio to a remote speaker or audio system is mounted at the top of the card.

Also available, on either cassette or 5-inch disk, is *Americana Plus*, 14 tunes including "The Entertainer" and Chopin's "Minute Waltz." The cassette version of *Americana Plus* is compatible with Percom's CIS-30+ cassette and data terminal interface unit and the SwTPC AC-30 unit. The disk version runs on Percom's LFD-400 system using MINIDOS-PLUSX. The *Americana Plus* programs are in machine language and do not require an assembler or interpreter program.

The Music Board sells for $59.95 assembled and tested. The cassette version of *Americana Plus* (MC-1SW) is priced at $15.95, and the disk version (MD-1PC) is $19.95. For further information, contact Percom Data Co, 211 N Kirby, Garland TX 75042.

Circle 533 on inquiry card.



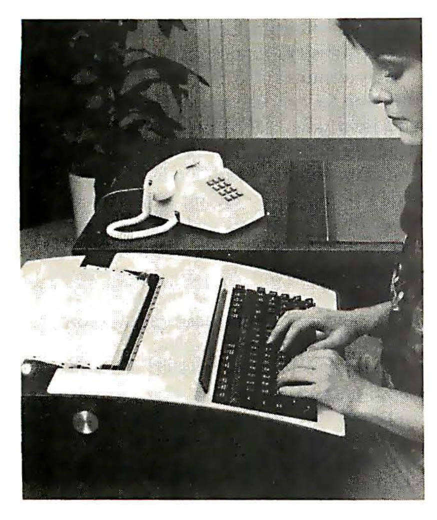


Thermal Strip Printer

The Model STSP-1 is a serial thermal strip printer which responds to an ASCII input by printing uppercase 5 by 7 dot matrix characters on a narrow paper strip. Originally designed for use with portable battery-powered items, the control circuit uses CMOS integrated circuits for low power consumption. The mechanism has only one moving part, and the printing process is silent. The last fifteen characters can be easily seen in the viewing area of the paper cassette. The parallel input port is at 5 V CMOS level. A busy line is provided to simplify interfacing.

The STSP-1 mechanism with control interface is priced at $225; the STSP-1E mechanism with control interface, enclosure, power supply, and input cable sells for $295; and a package of ten thermal print tape cassettes is $25. For further information, contact Prentke Romich Co, RD 2, POB 191, Shreve OH 44676. Circle 535 on inquiry card.

Buffered Tabletop Teleprinter



Teletype Corp has announced a tabletop buffered teleprinter featuring a microprocessor-based controller. The teleprinter comes with a send, edit and receive buffer, and with extensive user-activated options that make it attractive for a variety of applications. The tabletop Model 43 BSR (buffered send/receive) provides 16 K characters of solid-state storage. It can automatically send and receive data via its buffer at up to 180 characters per second. Simultaneously, data can be entered and edited off-line for future transmission.

The 43 BSR is designed for switched network timesharing and message switching applications where it can reduce transmission costs and computer connect time. The 43 BSR is also ideal for data base inquiry systems where several inquiries can be entered into the buffer off-line and then automatically sent to the host computer, which sends back information after each inquiry.

The price of the 132-column pin-feed teleprinter with 16 K buffer is $2483. In an 80-column friction feed configuration, the price is $2505. For further information, contact Teletype Corp, 5555 Touhy Ave, Skokie IL 60077.

Circle 534 on inquiry card.

Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgement the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

What's New?

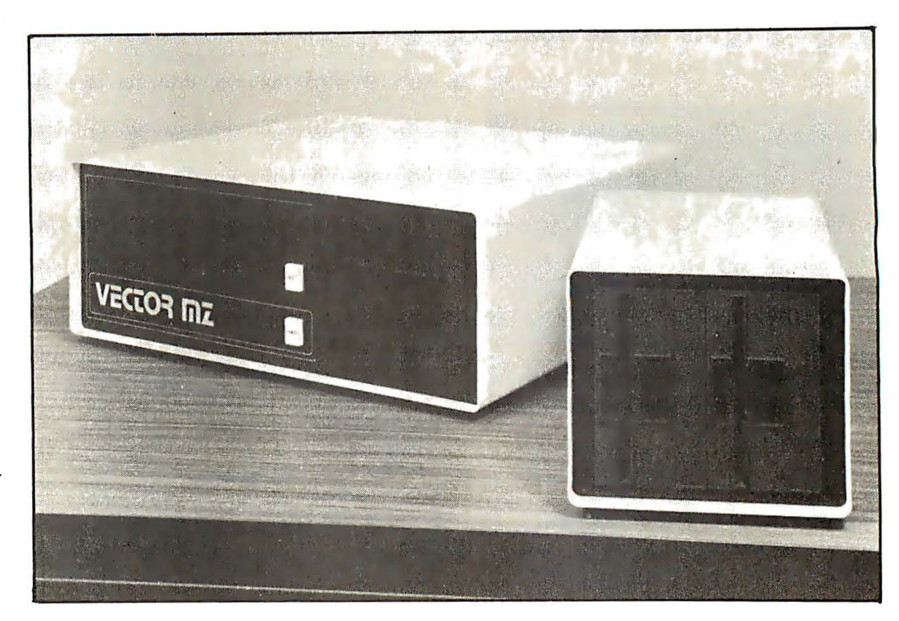
PERIPHERALS

Disk Module Doubles Disk Storage of Vector Graphic Systems

A 630,000 character dual floppy disk module has been announced by Vector Graphic Inc, 31364 Via Colinas, Westlake Village CA 91361. Called MICRO-STOR, this unit is used to expand Vector Graphic MZ and Memorite II systems from 2 to 4 disk drives. The unit features 2 Micropolis MOD II quad-density disk drives in an attractive chassis, using the standard 5-inch, 16-sectored disk. The module simply plugs into the existing disk controller board. The operating systems presently in use on Vector Graphic hardware were prepared in advance to make use of 4 drives.

Tested and assembled, the MICRO-STOR is priced at $1395.

Circle 525 on inquiry card.



Intelligent Printer Features 96-Character Set



The Trendcom 100 Intelligent Printer provides the microcomputer user with 40-column hard copy on 4½ inch (11.43 cm) wide paper. Interfaces are available for TRS-80, Apple II, PET and Sorcerer computers. The Trendcom 100 features bidirectional 40 character per second printing with a full 96-character ASCII set, including upper and lowercase letters, numerals, and punctuation marks. The 5 by 7 dot matrix characters are printed with either black or blue images, depending upon the paper used. The microprocessor-controlled unit is quiet, since it uses no print hammers, gears, or drive belts. This new printer uses a thick film thermal printhead to eliminate wear and reliability problems.

The Trendcom 100 is fully enclosed in a metal and high-impact plastic case and is available in both 115 V and 230 V AC versions. The printer is priced at $375. For further information, contact Trendcom, 484 Oakmead Pky, Sunnyvale CA 94086.

Circle 526 on inquiry card.

Four Printers from Dataroyal

These versions of the IPS-7000 series feature a 9-wire print head, a 7 by 9 dot matrix with full lowercase descenders, a 96 American Standard Code for Information Interchange (ASCII) character set that prints at 200 characters per second, and includes an 8-bit microprocessor. Models 7048 and 7248 feature a 500-character circular buffer, and Models 7049 and 7249 offer a 3500 character buffer. The new models include programmable vertical format control, an audible alarm, and a self-test switch.



The 7048 serial and 7248 parallel models are $1594, and the 7049 serial and 7249 parallel models are $1669. For further information, contact Dataroyal Inc, Main Dunstable Rd, Nashua NH 03061.

Circle 527 on inquiry card.

New Terminal Supports Data Processing and Word Processing Applications



The Hazeltine 1420 computer terminal is designed to support small business systems using both data and word processing software. It features a typewriter-style keyboard arrangement with both upper and lowercase, making it suitable for fast and accurate entry, and high-intensity blink or nondisplay (zero intensity) modes.

The terminal also features a program-function key mode as well as column and field tabs. All of the basic elements needed for up-to-date, fast data entry and data inquiry are included in the video terminal, including an enhanced separate numeric keypad. The Hazeltine 1420 operates with a standard EIA RS-232 interface with eight transmission rates up to 9600 bits per second (bps) which are switch selectable and accommodate all 128 ASCII codes.

The microprocessor design of the terminal permits utilization of fewer parts and increases its dependability. Its state-of-the-art design results in cool operating temperatures and makes possible the elimination of a fan.

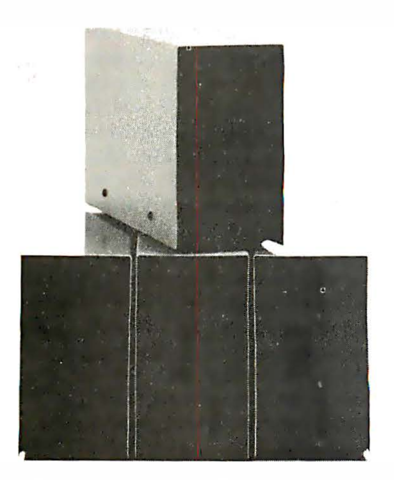
For further information, contact Hazeltine Corp, Computer Terminal Equipment, Greenlawn NY 11740.

Circle 528 on inquiry card.

What's New?

PERIPHERALS

Add-on Disk Drives for TRS-80

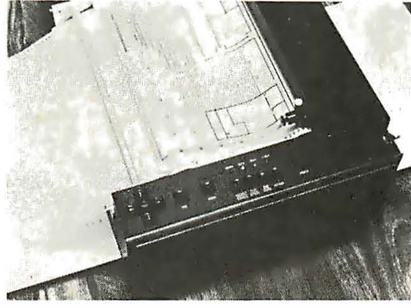


A family of add-on disk drives for the TRS-80 has been introduced by Microcomputer Technology Inc, 2080 S Grand Ave, Santa Ana CA 92705. The MTI single-head disk drive family (TF-X) offers the user a choice of MPI, Pertec, or Shugart SA400 5-inch floppy disk drives. The Shugart drive is the same device offered by Radio Shack, while the Pertec provides quieter operation and the use of both sides of the disk. The MPI unit provides additional features normally found in the 8-inch size disk drives, such as door lock and automatic disk ejection.

Prices for the TF-X single-head units start at $379. MTI's dual-headed units (TDH-X) provide the same capacity as two single-headed drives and are priced at $675.

Circle 529 on inquiry card.

Pen Plotter with Built-in Microcomputer-Based Controller



The Model 1553 is a compact, portable, desktop Digital Incremental Plotter with an integral microcomputer-based controller. The built-in RS-232 interface provides for on-line, off-line or remote operation via communication lines, as a timeshared terminal.

The unit's high speed (10 inches per second (ips) along axes, 14.14 ips diagonal movement) and the intelligence of the controller (hardware symbol and character generation, circle and arc generation, dot and dash generation, scale and rotate), make it suited for business graphics, process control and scientific analysis plotter applications. The resolution is 0.0025 inch for excellent line quality. A universal pen holder and dynamic adjuster allow the use of ballpoint, liquid roller, and fiber tip pens. Pen type and color changes can be accomplished easily during a plot through programmable plotter pause commands.

The price of the Digital Incremental Plotter is $5950. For further information, contact Nicolet Zeta Corp, 2300 Stanwell Dr, Concord CA 94520.

Circle 531 on inquiry card.



Microprocessor-Based Cassette Terminal Features NCR Compatibility

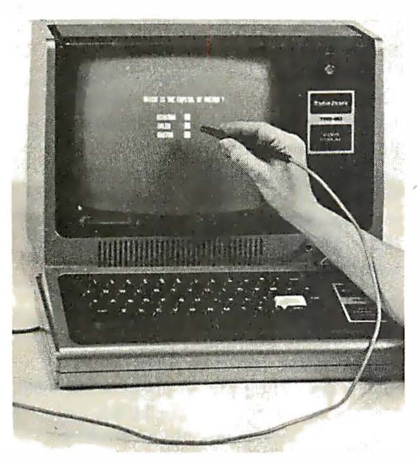
This NCR-compatible, microprocessor-based cassette terminal is for applications including data communications, data logging, and program loading. The MFE Model 5450VRL Microprocessor Cassette Terminal is an 8080-based data storage system that features an optional variable record length read capability for compatibility with NCR's variable block length systems. The standard 5450 is compatible with Sweda, Texas Instruments, and all other RS-232-compatible systems. Accommodating ANSI/EMCA-compatible cassettes, all MFE terminals automatically perform read after write, cyclic redundancy check, and parity error checks to insure data integrity.

The storage capacity for the MFE 5450VRL varies with record length; for the 5450, capacity is 442 K formatted characters. The MFE product line also includes the Model 5000 (221 K characters), and the 2500 (350 K characters). All, except the 2500, incorporate high-speed skip, search, and edit capability. The terminals operate in full and half duplex modes; full duplex provides echoplex operation for each character. Dual RS-232C I/O (input/output) interfaces are standard; 20 mA current loop is optional.

MFE Microprocessor Cassette Terminals are priced from $1995 each for the 5000 and 5450, and from $1190 for the 2500; the VRL option for the 5450 is $200. For further information, contact MFE Corp, Keewaydin Dr, Salem NH 03079.

Circle 532 on inquiry card.

Light Pen for Radio ShackTRS-80



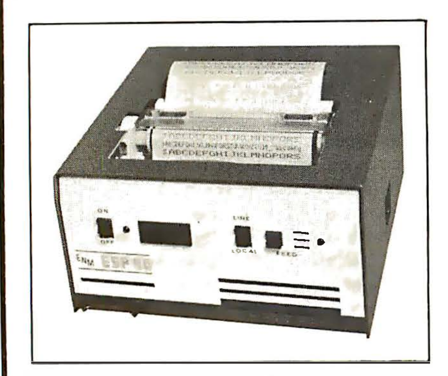
This self-contained light pen which plugs directly into the TRS-80 bus connector has been announced by the 3G Company Inc, Rt 3, POB 28a, Gaston OR 97119. The light pen makes it possible to bypass the TRS-80's keyboard and interact directly with the information displayed on the video screen. The light pen adds versatility to most graphics programs and makes possible unique games. A menu can be displayed on the screen, and the user can make a selection from that menu by using the light pen. This type of interaction makes it easy for the person who is not familiar with computers to use an applications program.

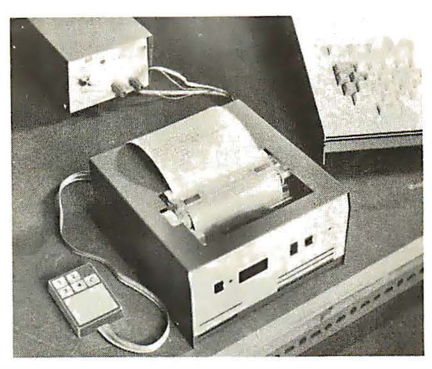
The light pen is completely assembled and ready to plug into the TRS-80. A sample program and programming instructions are included with the pen. The light pen sells for $34.95 plus $1.50 for postage and handling within the US ($6 for foreign orders). The pen includes a 30-day unconditional money back guarantee.

Circle 530 on inquiry card.

What's New?

PERIPHERALS





Miniature Printer Prints Text and Graphics

Called the ESP-40, this miniature printer can print images transmitted by digital facsimile equipment or can be used with any keyboard to form a low-cost printer terminal. The ESP-40 utilizes a nonimpact matrix printing process, and prints on electrosensitive paper 4 inches (10.16 cm) wide at rates up to 280 characters a second. A built-in microprocessor with a 320-character buffer memory enables the unit to print upper and lowercase characters (7 or 9 dots high) in a variety of styles and widths under program control. Between 5 and 20 characters per inch can be printed, and characters of different widths can be printed on the same line.

For plotting diagrams, the buffer output is applied directly to the printhead. This enables up to 8 vertical dots to be printed at 240 printhead positions across the width of the paper, and in this mode the line shift is 8 dots high. The unit can plot curves and circles with great accuracy, and produce maps, drawings, and copies of photographs as well as diagrams. The printing mechanism is controlled by a timing disk which synchronizes the printhead with the data buffer. This ensures that the quality of printing is unaffected by changes in voltage or in mechanical friction.

The ESP-40 is 8 by 8.3 by 4.1 inches (20.32 by 21.08 by 10.41 cm) without the cooling fan. An electronic watchdog monitors all functions and sounds an alarm in case of impending or actual failure. Used with a hand-held keypad, test routines for fault diagnosis are provided by the on-board software. For further information, contact English Numbering Machines Ltd, Printer Div, Queensway, Enfield EN3 4SB, Middlesex, ENGLAND.

Circle 536 on inquiry card.

New Terminal Fully Compatible with DEC VT-100



The DT80/1 video terminal offers full compatibility with Digital Equipment Corporation's VT-100. A key feature of the DT80/1 is its ability to interface with a printer in three different modes: on-line as data arrives; as a printer controller; and as a source for feeding data from the screen directly to the printer. The terminal offers a special display tube saver and self-diagnostics, and is protected by a one-year warranty.

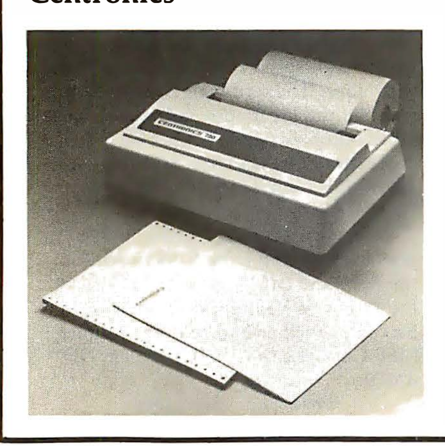
For optimum space flexibility, the DT80/1 has a detachable keyboard. The capacity of its video screen is 24 lines by 80 or 132 characters, with light-emitting diode indicators for operator awareness and status. The DT80/1 screen also offers such functions as underline, blink, and dual-intensity. In addition, the user may employ a split screen, double-high or double-wide characters, composite video input and output, and limited graphics. Reverse video is also keyboard selectable.

Other user convenience features include a typewriter-style keyboard, fixed and settable tabs, and bidirectional smooth scrolling. Internally, the DT80/1 houses a large-scale integrated technology video controller with two serial I/O (input/output) ports, which operate asynchronously with either RS-232C or 20 mA current loop. Communication speeds are up to 19,200 bits per second (bps).

For more information, contact Datamedia Corp, 7300 N Crescent Blvd, Pennsauken NJ 08110.

Circle 537 on inquiry card.

New Printers from Centronics



Centronics printers, Models 730-1 through 730-7, include such features as 50 character per second print speed, 80 column line length at 10 characters per inch (3.9 characters per cm), a full line buffer, high-speed carriage return, and 7 by 7 dot matrix printing. Each unit has a built-in tear bar for paper tear off within five lines of print and is capable of making three simultaneous copies.

The printers' typewriter-like platen takes hand fed 8.5 inch (21.6 cm) wide sheets in letter, legal size or longer lengths, standard international sized A4 sheets, and the fixed pins on the platen accept standard computer grade multipart or single-part fanfold paper 9 inches (23 cm) wide from pin-to-pin. This system also allows the use of 8.5 inch (21.6 cm) wide roll paper up to 5 inches (12.7 cm) in diameter.

The Model 730s can handle payroll checks on preprinted forms, inventory listings on computer-grade fanfold paper, direct-mail letters on cut sheets and general information on roll paper. Some other applications include electronic mail, message logging, technical and scientific data logging and reservation systems.

These units weigh less than 10 pounds (4.5 kg) and measure 14.5 inches (36.8 cm) wide by less than 12 inches (30.5 cm) deep and less than 5 (12.7 cm) inches tall. The parallel printers are $995 and the serial printers are $1045. Contact Chuck Clemente or Sterling Hager at Centronics, Hudson NH 03051.

Circle 538 on inquiry card.



SOFTWARE

Pascal Business Software

A fully integrated system of Pascal business accounting packages has been announced by PS inc, Fargo ND. Standardized on the UCSD implementation of the language, the software includes a general ledger package that permits a company to name and number over 1000 of its own accounts, and to generate financial reports for the overall operation and for separate profit centers. Accounts payable with aging and cash requirements reporting; accounts receivable with aging and sales analysis; order entry; and inventory control are all tied into the general ledger. It is menu-oriented for ease of training and use.

PS inc can supply their software on floppy disk or cartridge disk media.

For more information, contact PS inc, 619 NP Ave, Fargo ND 58102.

Circle 551 on inquiry card.

Macroassembler and Text Editor for PET, Apple II or SYM

The 6502 Macroassembler and Text Editor (ASSM/TED) is written specifically for the PET, Apple II, and SYM microcomputers. This software package was written in assembly language and occupies 8 K bytes of memory starting at hexadecimal location 2000. ASSM/TED provides 27 commands and 20 pseudo operations. Specific features include macroinstructions and conditional assembly support; extensive text editing commands (which include automatic line numbering, and string search and replace); tape load; record and append commands; vectors for interfacing to disk systems; free format source input; source-code syntax similar to MOS Technology specifications, and other functions.

The user manual and cassette tape in either PET, Apple II or SYM (HS) format are available for $35 plus $2 for shipping and handling. For further information, contact C W Moser, 3239 Linda Dr, Winston-Salem NC 27106.

Circle 552 on inquiry card.

Pascal for North Star Horizon

North Star Computers Inc has announced that Pascal is now available for use with the North Star Horizon computer and Micro Disk System (MDS). North Star Pascal incorporates the complete UCSD Pascal program development system. North Star's version of Pascal includes such standard language features as the four elementary data types: real and integer numbers, boolean (true and false), and char (characters). The programmer may also define custom data types. Both elementary and programmer-defined data types may be organized into arrays, records, sets, or sequential files.

Pascal programs are easily understandable since descriptive names may be given to variables, constants, procedures, and functions within a program. Several types of loops and two conditional statements are provided to control program execution. A restricted form of GOTO is also available. In addition, North Star Pascal includes several extensions which ease the task of writing major business and personal programs.

The North Star Pascal package includes its own operating system. Pascal programs are compiled into fast executing p-code and are executed at runtime by a program which simulates the operation of a hypothetical computer called the P-machine. The program development system is available on two single-density 5-inch disks or one double-density disk. Software provided with the system includes the P-machine simulator, Pascal operating system, Pascal compiler, and a screen-oriented text editor. A line-oriented text editor is also included with the system for use in situations where a suitable video terminal is not available.

For advanced applications, an auxiliary Pascal software package is available, containing a special assembler and numerous utility programs. With the assembler, it is possible to generate machine code procedures and functions which may be linked into compiled Pascal programs prior to execution. The auxiliary Pascal software package supplements the primary package described above.

The primary North Star package is $49 including reference manual. The auxiliary software package is available for $29. In ordering either package, specify whether single-density or double-density disk operation is desired. The system documentation package alone may be ordered for $20. For further information, contact North Star Computers, 2547 Ninth St, Berkeley CA 94710.

Circle 553 on inquiry card.

Development and Debugging Software for 6800 Microcomputer Programming

Percom Data Co has expanded its 6800 microcomputer software products line to include additional support programs for use in program development and debugging. The six programs that have been added include an assembler-linking loader, three disassemblers, a relocator, and a monitor with debugging conveniences. The programs are available on either cassette or disk, except the monitor which is in erasable read-only memory. Cassettes are Kansas City standard format at 300 bits per second (bps). The programs work with Percom operating systems. For prices and detailed description of the programs, write to Percom Data Co, 211 N Kirby, Garland TX 75042.

Circle 554 on inquiry card.

Software Packages for the USCD Pascal Operating System

Two new software packages are available for the UCSD Pascal operating system. The first package, FORMOUT, is a collection of routines to do formatted output from Pascal programs. Included routines allow formatted printing of strings and numbers, tabbing to a specific column, and printing an arbitrary number of spaces or some other printing character. FORMOUT allows the user to easily switch from one I/O (input/output) device to another so that programs can be switched between devices during processing.

CPMREAD, the second package, translates CP/M disk files to Pascal text files. It allows the user to investigate the CP/M disk directory and choose the files to be translated. Assembler and BASIC source code can be brought across and then modified for use on the Pascal system using the standard Pascal editors. Since CMPREAD is written completely in Pascal, it can run on any machine running the UCSD Pascal system, allowing LSI-11 (and other) systems to have access to CP/M files.

FORMOUT is available as a source listing with manual for $20. A machine-readable copy of FORMOUT is available on an 8-inch soft-sectored, single-density disk, for an additional $10. CPMREAD is distributed as an executable code file only and is available for $25. For further information, contact Pickles and Trout, POB 1206, Goleta CA 93017.

Circle 555 on inquiry card.

What's New?

SOFTWARE

Tiny Pascal for TRS-80

A compact version of Tiny Pascal fits in the standard 16 K byte TRS-80 system and consists of the compiler, text editor, runtime routines, p-code interpreter (which saves storage space), and a system monitor. Execution speed is about 4 times faster than Level II BASIC using integer variables. This verison is available from SuperSoft, POB 1628, Champaign IL 61820 for $40.

Circle 556 on inquiry card.

Software for Texas Instruments

This software system is written in BASIC, works on floppy and hard disk systems and includes inventory control, order entry, sales analysis, general ledger, accounts payable, accounts receivable, and payroll.

Some of the capabilities of this software include invoice printing; back order reports; sales analysis by salesmen, customer, and product; purchase order journals and much more.

This system works on the Texas Instruments 990 and 771 computers. It is available from Kitzmiller Systems, 252 S Oxford Ave, Los Angeles CA 90004.

Circle 557 on inquiry card.

Digital Research Introduces CP/M 2.0 and MP/M

Digital Research has announced two new disk operating systems that are adaptable to nearly any 8080 or Z80 computer system with disk backup storage. CP/M 2.0, an enhanced version of CP/M, release 1, can run simple floppy disk systems to large-capacity hard disk drives. Configuration is accomplished through a disk definition table which drives the file management algorithms, allowing simple field alteration.

MP/M is a CP/M compatible multiterminal operating system which supports real-time multiprogramming at each terminal, along with background and foreground modes. It can serve as a complete program development environment for one or more users, or as the nucleus of clustered terminals or processors accessing a common data base. MP/M device drivers can be altered in the field to operate with interrupt driven or polled I/O (input/output) devices.

CP/M 2.0 is $150 and MP/M is $300, which includes documentation and floppy disk in single-density 8-inch form. Contact Digital Research, POB 579, Pacific Grove CA 93950.

Circle 558 on inquiry card.

8080 Simulator and Debug Package for Apple II

The Apple-80 is an 8080 simulator and debug package designed for the 6502-based Apple II computer. It allows any 16 K byte or larger Apple II to run programs written for the 8080, and can be used as a design and debugging aid for the development of original 8080 software.

Apple-80 provides single step, trace, and run modes, and executes all valid 8080 op codes. Illegal op codes are rejected. All 8080 registers are visible on the Apple screen and may be modified at will. 8080 I/O (input/output) port addresses are arranged in a table for ease of user modification. Up to eight breakpoints may be set to facilitate program debugging. 6502 subroutines may be called directly from 8080 programs, allowing full access to Apple monitor and user-written functions. Conversely, 8080 routines may be embedded in 6502 programs. Vectored interrupts are also simulated.

The complete Apple-80 package includes Apple-80 routines, a manual, an 8080 program which demonstrates Apple-80 features, and an Apple-80 ready-reference card. The package is priced at $20 plus $1.50 for shipping and handling. For further information, contact Dann McCreary, POB 16435-B, San Diego CA 92116.

Circle 559 on inquiry card.

Text Output Processor

Script-80 is an 8080 microcomputer-based text output processing program that is compatible with the Script text processors available on most large mainframe computers. Developed to handle form letters, document files, and mailing lists, Script-80 requires an 8080 or Z80-based microcomputer with at least 16 K bytes of memory, a printer or hard copy terminal, a floppy disk drive, and CP/M or a compatible (CDOS, IMDOS, etc) operating system. The Script-80 system supports over 50 standard Script commands for the combining of multiple files, formatting and right-justifying of text, margin and line length control, centering of title lines, spacing, immediate and conditional page eject, page headings, page footings, and several formats of page numbering. Text from up to 255 files may be nested and embedded in the ouput text as though they are a part of the original file. Additional features include picture (pixel) processing, automatic multidisk search for embedded files, and extended upper and lowercase conversion capabilities.

The Script-80 Professional version extends page, multiple disk, and output device handling. The user's manual explains how to use Script-80 with BASIC for selective mailing of form letters. The Commercial version goes beyond the Professional version to support mass personalized-letter mailing techniques.

The single-drive Hobbyist version is $45; the multidrive Professional version sells for $125; the full Commercial version with two-year update and maintenance service is $625; the manual alone (specify version) is priced at $25. For further information, contact J Vilkaitis Consultants, POB 26, 417 High St Ext, Thomaston CT 06787.

Circle 560 on inquiry card.

Apple Releases New Software

Apple Computer Co has released volumes 3 through 5 of the *Apple Software Bank*, a library of user-contributed programs. The new programs include File Cabinet, a personal directory and record keeping system; Character Generator, a program to label high-resolution graphic images; California Driver's Test, (a simulation of the actual exam); Integer Basic Renumber/Append; and 25 others.

Accompanying the 3 new volumes is a 90-page manual providing detailed descriptions and operating instructions for each of the programs. Called the *Bonus Issue*, the manual is an effective aid for Apple II users trying to establish or improve good programming techniques.

Apple also introduced 2 new graphics-oriented games, Apple Bowl and Microchess. Both games use high-resolution graphics. Apple Bowl creates a life-like simulation of bowling, including ball speed and spin control capabilities to help bowlers perfect their games. Microchess is a strategy game and includes 8 levels of ability, from which the user can select the one most closely matching their playing skill.

The *Apple Software Bank* user-contributed programs are available from Apple dealers. Users must provide their own blank disk or cassette tape for copying the programs. A copy fee of $10 per disk or $2 per program is charged. The *Bonus Issue* manual is free with the purchase of all or any programs. Microchess is priced at $20 on cassette and $25 on disk, and Apple ·wl Bowl is priced at $20 on cassette or disk. For further information, contact Apple Computer Inc, 10260 Bandley Dr, Cupertino CA 95014.

Circle 561 on inquiry card.

Circle 126 on inquiry card.

The DATA-TRANS 1000

A completely refurbished **IBM** Selectric Terminal with built-in **ASCII** Interface.

$1395



Features:

- 300 Baud
- 14.9 characters per second printout
- Reliable heavy duty Selectric mechanism
- RS-232C Interface
- Documentation included
- 60 day warranty - parts and labor
- High quality Selectric printing Off-line use as typewriter
- Optional tractor feed available
- 15 inch carriage width



HOW TO ORDER DATA-TRANS 1000

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2. All orders are shipped F.O.B. San Jose, CA
3. Deliveries are immediate

For orders and information

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2154 O'Toole St.
Unit E
San Jose, CA 95131
Phone: (408) 263-9246

MICRO-PROCESSORS: FROM CHIPS TO SYSTEMS

This book cover all aspects of microprocessors, from the basic concepts to advanced interfacing techniques, in a progressive presentation. It is independent from any manufacturer, and presents uniform **standard** principles and design techniques, including the interconnect of a **standard** system, as well as specific components. It introduces the MPU, how it works internally, the system components (ROM, RAM, UART, PIO, others), the system interconnect, applications, programming, and the problems and techniques of system development. By R. Zaks. SYBEX. Ref. C201. $9.95

MICRO-PROCESSOR INTERFACING TECHNIQUES

Microprocessor interfacing is no longer an art. It is a set of techniques, and in some cases just a set of components. This comprehensive book introduces the basic interfacing concepts and techniques, then presents in detail the implementation details, from hardware to software. It covers all the essential peripherals, from keyboard to floppy disk, as well as the standard buses (S100 to IEEE 488) and introduces the basic troubleshooting techniques. (2nd Expanded Edition). By Austin Lesea and R. Zaks. Ref. C207 SYBEX. $11.95

PROGRAMMING THE 6502 PROGRAMMING THE Z80 PROGRAMMING THE 8080*

It covers all essential aspects of programming, as well as the advantages and disadvantages of the 6502 and should bring the reader to the point where he can start writing complete applications programs. For the reader who wishes more, a companion volume is available: The 6502 Applications Book. By R. Zaks. 6502: Ref. C202; Z80: Ref. C280; 8080: Ref. C208. SYBEX. Each $10.95



44 BUS MOTHER BOARD

Has provisions for ten 44 pin (.156) connectors, spaced 3/4 of an inch apart. Pin 20 is connected to X, and 22 is connected to Z for power and ground. All the other pins are connected in parallel. This board also has provisions for bypass capacitors. Board cost $15.00 Part No. 102. Connectors $3.00 each Part No. 44WP.



AN INTRODUCTION TO PERSONAL AND BUSINESS COMPUTING

No computer background is required. The book is designed to educate the reader in all the aspects of a system, from the selection of the microcomputer to the required peripherals. By Rodnay Zaks. Ref. C200, SYBEX $6.95

TVT COOKBOOK

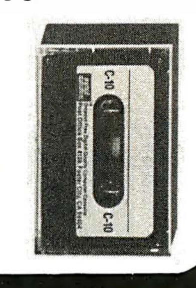
Bk 1064 — by Don Lancaster. Describes the use of a standard television receiver as a microprocessor CRT terminal. Explains and describes character generation, cursor control and interface information in typical, easy-to-understand Lancascaster style. $9.95

COMPUTER PROGRAMMING HANDBOOK

A complete guide to computer programming & data processing. Includes many worked-out examples. By Peter Staak, TAB $9.95

DIGITAL CASSETTE

5 min. each side. Box of 10 $9.95. Part No. C-5.



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COMPUCRUISE

Put a computer in your car, which gives you the most effective and functional cruise control ever designed, plus complete trip computing, fuel management systems, and a remarkable accurate quartz crystal time system.

So simple a child can operate, the new CompuCruise combines latest computer technology with state-of-the-art reliability in a package which will not likely be available on new cars for years to come • Cruise Control • Time, E. T., Lap Timer, Alarm • Time, Distance, Fuel to Arrival • Time, Distance, Fuel to Empty • Time, Distance and Fuel on Trip • Current or Average MPG, GPH • Fuel Used, Distance since Fillup • Current and Average-Vehicle Speed • Inside, Outside or Coolant Temperature • Battery Voltage • English or Metric Display. $199.95, without cruise control $159.95.



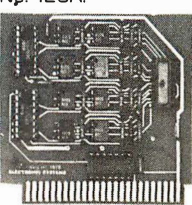
FLOPPY DISK STORAGE BINDER

This black vinyl three-ring binder comes with ten transparent plastic sleeves which accommodate either twenty, five-inch or ten, eight-inch floppy disks. The plastic sleeves may be ordered separately and added as needed. A contents file is included with each sleeve for easy identification and organizing. Binder & 10 holders $14.95 Part No. B800; Extra holders 95¢ each. Part No. 800



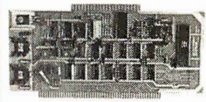
OPTO-ISOLATED PARALLEL INPUT BOARD FOR APPLE II

There are 8 inputs that can be driven from TTL logic or any 5 volt source. The circuit board can be plugged into any of the 8 sockets of your Apple II. It has a 16 pin socket for standard dip ribbon cable connection.
Board only $15.00. Part No. 120, with parts $69.95. Part No. 120A.



TIDMA

• Tape Interface Direct Memory Access • Record and play programs without bootstrap loader (no prom) has FSK encoder/decoder for direct connections to low cost recorder at 1200 baud rate, and direct connections for inputs and outputs to a digital recorder at any baud rate • S-100 bus compatible • Board only $35.00 Part No. 112, with parts $110 Part No. 112A

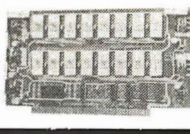


SYSTEM MONITOR

8080, 8085, or Z-80 System monitor for use with the TIDMA board. There is no need for the front panel. Complete with documentation $12.95.

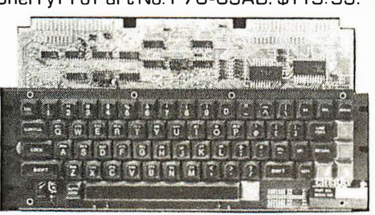
16K EPROM

Uses 2708 EPROMS, memory speed selection provided, addressable anywhere in 65K of memory, can be shadowed in 4K increments. Board only $24.95 part no. 7902, with parts less EPROMs $49.95 part no. 7902A.



ASCII KEYBOARD

TTL & DTL compatible • Full 67 key array • Full 128 character ASCII output • Positive logic with outputs resting low • Data Strobe • Five user-definable spare keys • Standard 22 pin dual card edge connector • Requires +5VDC, 325 mA. Assembled & Tested. Cherry Pro Part No. P70-05AB. $119.95.



ASCII KEYBOARD

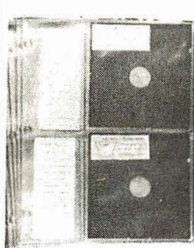
53 Keys popular ASR-33 format • Rugged G-10 P.C. Board • Tri-mode MOS encoding • Two-Key Rollover • MOS/DTL/TTL Compatible • Upper Case lockout • Data and Strobe inversion option • Three User Definable Keys • Low contact bounce • Selectable Parity • Custom Keycaps • George Risk Model 753. Requires +5, -12 volts. $59.95 Kit.

ASCII TO CORRESPONDENCE CODE CONVERTER

This bidirectional board is a direct replacement for the board inside the Trendata 1000 terminal. The on board connector provides RS-232 serial in and out. Sold only as an assembled and tested unit for $229.95. Part No. TA 1000C

DISK JACKET™

Made from heavy duty .0095 matte plastic with reinforced grommets. The minidiskette version holds two 5-1/4 inch diskettes and will fit any standard three ring binder. The pockets to the left of the diskette can be used for listing the contents of the disk. Please order only in multitudes of ten. $9.95/10 Pack.



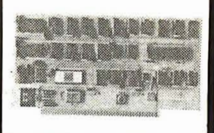
ATARI 800

Computer with 8K $995.00, disk drive $549.00, printer $599.99



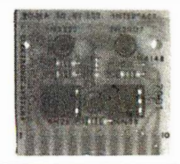
VIDEO TERMINAL

16 lines, 64 columns • Upper and lower case • 5x7 dot matrix • Serial RS-232 in and out with TTL parallel keyboard input • On board baud rate generator 75, 110, 150, 300, 600, & 1200 jumper selectable • Memory 1024 characters (7-21L02) • Video processor chip SFF96364 by Neculonic • Control characters (CR, LF, →, ←, ↑, ↓, non destructive cursor, CS, home, CL • White characters on black background or vice-versa • With the addition of a keyboard, video monitor or TV set with TV interface (part no. 107A) and power supply this is a complete stand alone terminal • also S-100 compatible • requires +16, & −16 VDC at 100mA, and 8VDC at 1A. Part No. 1000A $199.95 kit.



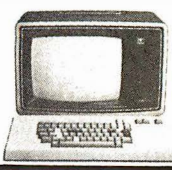
RS-232/20mA INTERFACE

This board has two passive, opto-isolated circuits. One converts RS-232 to 20mA, the other converts 20mA to RS-232. All connections go to a 10 pin edge connector. Requires +12 and -12 volts. Board only $9.95, part no. 7901, with parts $14.95 Part No. 7901A.



COMPUCOLOR II

Model 3, 8K $13 95, Model 4, 16K $15 95, Model 5, 32K $18 95. Prices include color monitor, computer, and one disk drive.



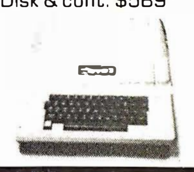
PET COMPUTER

With 32K & monitor - $1195. Dual Disk Drive - $1195.

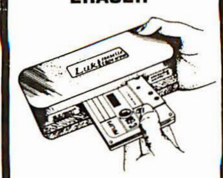


apple II or APPLE II PLUS

16K - **$979**, 32K - $1059, 48K - $1123. Disk & cont. $589



CASSETTE TAPE ERASER



REMOVES RECORDINGS IN ONE SECOND! The process eliminates static positive / negative ions and maintains original tone quality with minimal tape hiss • To improve tone quality • To reduce hissing • For quick and easy to erase • No battery or liquid required • Powerful and effective action • Unconditional 2 year guarantee. ERASER-8 $19.95.

16K RAMS

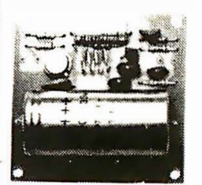
For the Apple, TRS-80 or Pet $8 each Part No. 4116/ 2117.

APPLE II HOBBY/ PROTOTYPING CARD

$14.95 Part No. 7907

T.V. INTERFACE

• Converts video to AM modulated RF, Channels 2 or 3. So powerful almost no tuning is required. On board regulated power supply makes this extremely stable. Rated very highly in Doctor Dobbs' Journal. Recommended by Apple • Power required is 12 volts AC C.T., or +5 volts DC • Board only $7.60 part No. 107, with parts $13.50 Part No. 107A





PARALLEL TRIAC OUTPUT BOARD FOR APPLE II

This board has 8 triacs capable of switching 110 volt 6 amp loads (660 watts per channel) or a total of 5280 watts. Board only $15.00 Part No. 210, with parts $119.95 Part No. 210A.

To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U. S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U. S. dollars. Dealer inquiries invited. 24 hour order line (408) 448-0800



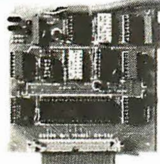
Send for FREE Catalog . . . a big self-addressed envelope with 41¢ postage gets it fastest!

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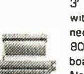
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TRS-80 E.S. SERIAL I/O

• Can input into basic • Can use LLIST and LPRINT to output, or output continuously • RS-232 compatible • Can be used with or without the expansion bus • On board switch selectable baud rates of 110, 150, 300, 600, 1200, 2400, parity or no parity odd or even, 5 to 8 data bits, and 1 or 2 stop bits. D.T.R. line • Requires +5, -12 VDC • Board only $19.95 Part No. 8010, with parts $59.95 Part No. 8010A, assembled $79.95 Part No. 8010 C. No connectors provided, see below.



EIA/RS-232 connector Part No. DB25P $6.00, with 9'. 8 conductor cable $10.95 Part No. DB25P9



3' ribbon cable withattachedconnectors tofit TRS-80 and our serial board $19.95 Part No. 3CAB40.

MODEM

• Type 103 • Full or half duplex • Works up to 300 baud • Originate or Answer • No coils, only low cost components • TTL input and output-serial • Connect 8 Ω speaker and crystal mic. directly to board • Uses XR FSK demodulator • Requires +5 volts • Board only $7.60 Part No. 109, with parts $27.50 Part No. 109A

DISKETTES

Box of 10, 5" $29.95, 8" $39.95.
Plastic box, holds 10 diskettes, 5" - $4.50, 8" - $6.50.

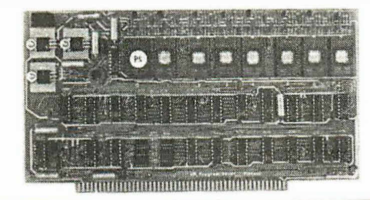
APPLE II SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

8K EPROM PIICEON

Saves programs on PROM permanently (until erased via UV light) up to 8K bytes. Programs may be directly run from the program saver such as fixed routines or assemblers. • S-100 bus compatible • Room for 8K bytes of EPROM non-volatile memory (2708's). • On-board PROM programming • Address relocation of each 4K of memory to any 4K boundary within 64K • Power on jump and reset jump option for "turnkey" systems and computers without a front panel • Program saver software available • Solder mask both sides • Full silkscreen for easy assembly. Program saver software in 1 2708 EPROM $25. Bare board $35 including custom coil, board with parts but no EPROMS $139, with 4 EPROMS $179, with 8 EPROMS $219.

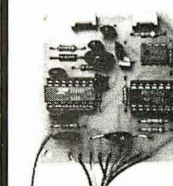


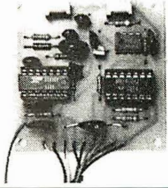
T.V. TYPEWRITER

• Stand alone TVT • 32 char/line, 16 lines, modifications for 64 char/line included • Parallel ASCII (TTL) input • Video output • 1K on board memory • Output for computer controlled curser • Auto scroll • Non-destructive curser • Curser inputs: up, down, left, right, home, EOL, EOS • Scroll up, down • Requires +5 volts at 1.5 amps, and -12 volts at 30 mA • All 7400, TTL chips • Char. gen. 2513 • Upper case only • Board only $39.00 Part No. 106, with parts $145.00 Part No. 106A

TAPE INTERFACE

• Play and record Kansas City Standard tapes • Converts a low cost tape recorder to a digital recorder • Works up to 1200 baud • Digital in and out are TTL-serial • Output of board connects to mic. in of recorder • Earphone of recorder connects to input on board • No coils • Requires +5 volts, low power drain • Board only $7.60 Part No. 111, with parts $27.50 Part No. 111A



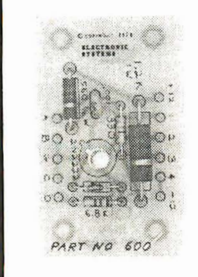


RS-232/ TTL INTERFACE

• Converts TTL to RS-232, and converts RS-232 to TTL • Two separate circuits • Requires -12 and +12 volts • All connections go to a 10 pin gold plated edge connector, kit $ 9.95 Part No. 232A 10 Pin edge connector $3.00 Part No. 10P.

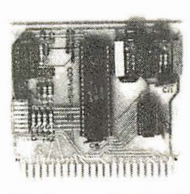
RS-232/TTY INTERFACE

This board has two active circuits, one converts RS-232 to 20mA, and the other converts 20mA to RS-232. Requires +12 and -12 volts. $9.95 Part No. 600A Kit.



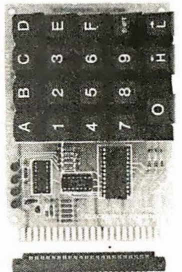
UART & BAUD RATE GENERATOR

• Converts serial to parallel and parallel to serial • Low cost on board baud rate generator • Baud rates: 110, 150, 300, 600, 1200, and 2400 • Low power drain +5 volts and -12 volts required • TTL compatible • All characters contain a start bit, 5 to 8 data bits, 1 or 2 stop bits, and either odd or even parity. • All connections go to a 44 pin gold plated edge connector • Board only $12.00 Part No. 101, with parts $35.00 Part No. 101A, 44 pin edge connector $4.00 Part No. 44P



HEX ENCODED KEYBOARD E.S.

This HEX keyboard has 19 keys, 16 encoded with 3 user definable. The encoded TTL outputs, 8-4-2-1 and STROBE are debounced and available in true and complement form. Four onboard LEDs indicate the HEX code generated for each key depression. The board requires a single +5 volt supply. Board only $15.00 Part No. HEX-3, with parts $49.95 Part No. HEX-3A. 44 pin edge connector $4.00 Part No. 44P.



WAMECO PRODUCTS WITH ELECTRONIC SYSTEMS PARTS

FDC-1 FLOPPY CONTROLLER BOARD will drive shugart, pertek, remex 5" & 8" drives up to 8 drives, on board PROM with power boot up, will operate with CPM (not included). PCBD $42.95

FPB-1 Front Panel. (Finally) IMSAI size hex displays. Byte or instruction single step. PCBD $42.95

MEM-1A 8Kx8 fully buffered, S-100, uses 2102 type RAMS. PCBD .... $24.95, $168 Kit

QMB-12 MOTHER BOARD, 13 slot, terminated, S-100 board only .... $34.95 $89.95 Kit

CPU-1 8080A Processor board S-100 with 8 level vector interrupt PCBD .. $25.95 $89.95 Kit

RTC-1 Realtime clock board. Two independent interrupts. Software programmable. PCBD .... $25.95, $60.95 Kit

EPM-1 1702A 4K EPROM card PCBD .... $25.95 $49.95 with parts less EPROMS

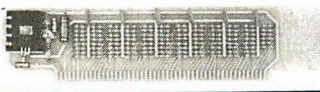
EPM-2 2708/2716 16K/32K EPROM card PCBD .... $24.95 $49.95 with parts less EPROMS

QMB-9 MOTHER BOARD. Short Version of QMB-12. 9 Slots PCBD .... $30.95 $67.95 Kit

MEM-2 16Kx8 Fully Buffered 2114 Board PCBD .... $25.95, $269.95 Kit

S-100 BUS ACTIVE TERMINATOR

Board only $14.95 Part No. 900, with parts $24.95 Part No. 900A



DC POWER SUPPLY

• Board supplies a regulated +5 volts at 3 amps., +12, -12, and -5 volts at 1 amp. • Power required is 8 volts AC at 3 amps., and 24 volts AC C.T. at 1.5 amps. • Board only $12.50 Part No. 6085, with parts excluding transformers $42.50 Part No. 6085A



To Order: Mention part no. description, and price. In USA shipping paid by us for orders accompanied by check or money order. We accept C.O.D. orders in the U.S. only, or a VISA or Master Charge no., expiration date, signature, phone no., shipping charges will be added. CA residents add 6.5% for tax. Outside USA add 10% for air mail postage and handling. Payment must be in U.S. dollars. Dealer inquiries invited. 24 hour order line (408) 448-0800

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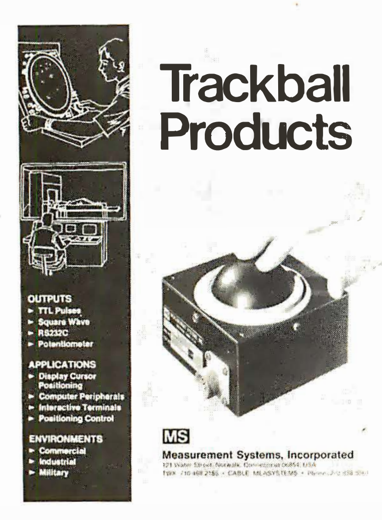
ELECTRONIC SYSTEMS Dept. B , P. O. Box 21638, San Jose, CA USA 95151

Circle 125 on inquiry card.

What's New?

PUBLICATIONS

New Trackball Products Catalog



Measurement Systems Inc has announced publication of their 12-page catalog of Trackball products. Trackballs are widely used for the human operator to perform positioning or contouring tasks on interactive displays either in computer peripherals or radar systems. Almost one half of the catalog contains technical and application data so that the reader gains a full understanding of this product. The balance of the catalog provides extensive data on specific standard items with options available. Fourteen trackballs are described, ranging in size from 2 to 3½ inches in diameter (5.08 to 8.89 cm). For further information, contact Measurement Systems Inc, 121 Water St, Norwalk CT 06854.

Circle 539 on inquiry card.

Free Apple Software Catalog from Rainbow

This 45-page catalog includes over 100 games of all types, fifteen business applications, twelve demonstration programs from voice recognition and speech synthesis to high-resolution and color graphics, and software development programs. Rainbow's "Pot O' Gold" of 49 games and demonstrations is also featured.

Prices for programs on cassette and diskette average around $10 to $20. Write Rainbow Computing Inc at 9719 Reseda Blvd, Northridge CA 91324 or call (213) 349-5560 for your free catalog.

Circle 541 on inquiry card.

PIPS for VIPS

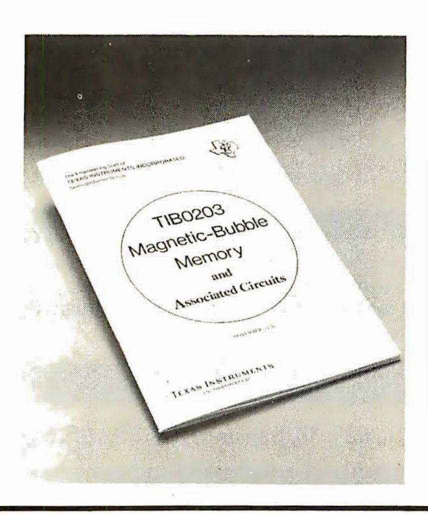
PIPS written by Tom Swan contains 160 pages of programs and documentation for use on the RCA COSMAC VIP, and an appendix describing modifications which can be made to allow the *PIPS* programs to be run on the ELF computers.

The first program, "Character Designer," facilitates building and editing a complete American Standard Code for Information Interchange (ASCII) and graphics character set, the remaining three programs use the display capabilities generated by the "Character Designer" to build text files. "Messager" allows easy text and graphics display from within CHIP-8; "Text Editor-21" is a general-purpose text editor, and "Disassembler-7" is an 1802 machine language disassembler. All these programs utilize a high-resolution display method described in *PIPS*. The remaining programs in the book are a "CHIP-8 Program Editor" and two games written in CHIP-8: Space Wars and Surround.

The book is available from Aresco, POB 1142, Columbia MD 21044, for $19.95. The price includes a companion cassette containing all the *PIPS* programs.

Circle 542 on inquiry card.

Free TIB0203 Data Book from Texas Instruments



A data book on the TIB0203 magnetic bubble memory has been announced by Texas Intruments Inc, POB 225012, Dallas TX 75265. The 48 page book, publication number LCC4430, contains complete specifications on the TIB0203 and, in addition, an 8 page discussion on the basic fundamentals and advantages of magnetic bubble memories. Also included in the manual are specification sheets for the interfacing integrated circuits which have been designed for use with the TIB0203. The additional data sheets include those for SN74LS361 function timing generator, SN75281 sense amplifier, SN75380 function driver, and SN75382 coil driver. Data sheets for standard devices which are needed for bubble memory system design, such as TSP102 thermistor and VSB53 Schottky-diode bridge, are also included.

Circle 540 on Inquiry card.

New Book Series on Computers

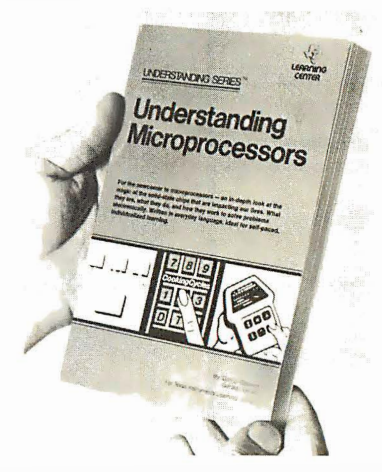
Academic Press Inc, 111 5th Ave, New York NY 10003, is publishing a series of books that cover a wide range of topics in the computer field.

Physics of Computer Memory Devices, Artificial Intelligence, Computer Vision Systems, Pattern Recognition and Artificial Intelligence, and *Associative Networks* are some of the books now on the market.

The prices range from $29 to $39.50

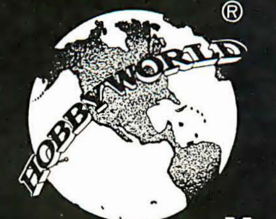
Circle 543 on inquiry card.

Book on Microprocessors from Texas Instruments



Written in nontechnical language, *Understanding Microprocessors* covers the aspects of microcomputer systems which use a microprocessor chip as the central unit for processing and control. This book provides the layman with the basics of what comprises a microprocessor, how it fits into the microcomputer system, what other system parts are necessary and how the microcomputer system functions. It introduces the reader to digital electronics, integrated circuit functions and includes 8- and 16-bit microprocessor applications with exercises and solutions. It is priced at $4.95 and is available from Texas Instruments Inc, POB 3640, MS 84, Dallas TX 75285.

Circle 544 on inquiry card.



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SSM PB1
2708/16 EPROM BOARD
• *S-100 Bus*
Programs eproms. Has provisions for 4K or 8K of eprom. With tex-tool sockets.
Cat No. 1440 PB1 kit $135

SSM AIO
SERIAL/ PARALLEL INTERFACE
• *Apple Bus*
One RS-232 serial, two bi-directional parallel. Interface your Apple to printers, plotters, terminals. With firmware, cables.
Cat No. 1918 AIO kit $129
Cat No. 1919 AIO a&t $169

SSM VB1B
VIDEO INTERFACE
• *S-100 Bus*
64 x 16 video, upper and lower case, greek. Composite and parallel video. White on black, or reverse.
Cat No. 1417 VB1B kit $129
Cat No. 1419 VB1B bbd $ 26

SSM IO4
2 SERIAL + 2 PARALLEL PORTS • *S-100 Bus*
Full handshaking, 20/60mA current loop. Dip switch address selection.
Cat No. 1411 IO4 kit $139
Cat No. 1413 IO4 kit $ 26

SSM CB1A
8080A CPU BOARD
• *S-100 Bus*
2K of PROM, 1K of RAM. Power on/reset, vector jump, parallel port with status.
Cat No. 2044 kit $155
Cat No. 2045 bbd $26

MARINCHIP M9900
16 BIT CPU
• *S-100 Bus*
Includes DOS, BASIC, word processor, text editor, assembler, linker, diagnostics and debug tools. Increases system performance by a factor of 2!

Cat No.	Description	Price
1379	M9900 CPU kit	$550
1950	as above, a&t	$700
1951	PROM/RAM/SIO kit	$275
1964	as above, a&t	$350
1940	PASCAL	$150
1941	META	$ 50
1942	System generation kit	$100
1943	Full documentation	$ 20

SSM CB2
Z-80(A) CPU BOARD
2 or 4 MHz, dip switch selectable. 2 sockets for 2716's or 2732 eproms or TMS4016 rams. MWRITE, firmware vector jump. Allows more than 64K ram.
Cat No. 2046 kit $199

SSM VB3
80 CHAR. VIDEO BOARD
• *S-100 bus*
80 char/line, 24 lines. upper & lower case, plus 256 user defined symbols, plus 160 x 204 graphics. Memory mapped. US and European campatible.
Cat No. 2047 2MHz kit $369
Cat No. 2049 4MHz kit $395

ITHACA
Z-80 CPU BOARD • *S-100 Bus*
2.5MHz or 4 MHz, on board 2708, optional MWRITE, allows operation without front panel.
Cat No. 1512 bareboard $32

ITHACA
2708/16 EPROM BOARD
Accepts up to 16 eproms. Dip switch adressable to any 1K location. Unused ROM locations may be allocated to RAM by dip switch.
Cat No. 1511 bareboard $28

TARBELL
CASSETTE INTERFACE
• *S-100 Bus*
Fastest transfer rate: 187 to 540 bytes/sec. Phase encoding (self-clocking). Generates Kansas City tapes.
Cat No. 1756 kit $120

TARBELL
32K STATIC RAM • *S-100 Bus*
Extended addressing (bank switching), phantom line, low power requirements. 9 on-board regulators!
Cat No. 1979 kit $625

TARBELL
FLOPPY DISK INTERFACE
• *S-100 Bus*
Up to 4 single drives in daisy chain. 250 bits per sec. Works with modified CPM and BASIC compiler. Build in phantom bootstrap.
Cat No. 1901 kit $190
Cat No. 1774 bareboard $ 40

SSM SB1
MUSIC SYNTHESIZER
• *S-100 Bus*
Freq range 15-20,000 Hz. Software uses only 4K RAM. Uses standard ASCII encoding for music encoding. Includes timer. Use more than one board for chords and harmonies.
Cat No. 1408 SB1 kit $145 (with software)
Cat No. 1410 SB1 bbd $35

SD SYSTEMS
VERSAFLOPPY
• *S-100 Bus*
Operates with Z-80, 8080(A), 8085. Controls up to four 5¼" or 8" drives. Dozens of features.
Cat No. 1516 kit $159

SD SYSTEMS
EXPANDORAM
• *S-100 Bus*
Interfaces with Sol, Altair, Imsai, Cromemco, etc. Expand dynamic memory in blocks of 8 to 64K. Dip switch selection for positioning boundaries. Write protect, phantom output disable. Uses 4116 rams.
Cat No. 1517-0 kit $185
Cat No. 1156-C 16K RAM $80ea

SD SYSTEMS
VIDEO DISPLAY BOARD • *S-100 Bus*
Interfaces a monitor and a keyboard to the S-100 Bus. On-board Z-80 controls functions. 80 x 24 display. 2K on-board RAM.
Cat No. 1599 kit $318

WAMECO QMB-12
12 SLOT MOTHERBOARD
• *S-100 Bus*
Very quiet! On-board kluge area accepts up to two 40-pin sockets. Also area for 3 separate voltages.
Cat No. 1507 bareboard $36

WAMECO FDC-1
FLOPPY DISK CONTROLLER
Controls up to eight Shugarts, Pertecs, Remex's, or MPI's. Also designed to operate with CPM software. Compatible with Z-80 or 8080 systems.
Cat No. 1377 bareboard $48

WAMECO FPB-1
FRONT PANEL BOARD
Similar to Imsai. Controls 8080A computer. Features memory examine, memory deposit, RUN, STOP, RESET. Hex displays. Byte or instruction single step.
Cat No. 1322 bareboard $47

CCS 7115A
APPLE II PROM MODULE
Add firmware without changing ROMs. 14K space available. Uses 5V 2716 eproms.
Cat No. 1630 kit $62
Cat No. 1631 a&t $72

CCS 7710A
APPLE II ASYNCHRONOUS SERIAL INTERFACE
Interfaces printers, etc. Features serial with full handshaking, and RS-232C (A thru E).
Cat No. 1623 kit $90
Cat No. 1624 a&t $145

CCS 7712A
APPLE II SYNCHRONOUS SERIAL INTERFACE
RS-232C (A thru E). Standard synchronous signalling rate per RS269/ANSI x3.1-1976.
Cat No. 1627 kit $90
Cat No. 1628 a&t $145

CCS 7520AK
APPLE II EXTENDER BOARD
Use for debugging or testing modules in the Apple II.
Cat No. 1611 kit $21

CCS 7720A
APPLE II PARALLEL INTERFACE
Interface printers and other peripherals. Programmable interrupt, 2 bi-directional ports, full handshaking.
Cat No. 1632 kit $62
Cat No. 1633 a&t $105

CCS 7470A
APPLE II BCD A/D CONVERTER
Single channel A/D, 12 bits. Allows conversion of −4 to +4 VDC to a BCD number, 200usec/conversion.
Cat No. 1621 kit $115
Cat No. 1622 a&t $135

CCS 2520A
EXTENDER/ TERMINATOR BOARD • *S-100 Bus*
Active and/or dynamic termination. Lebeled S-100 signals.
Cat No. 1610 kit $38

CCS MXVI
16K STATIC RAM MODULE
• *S-100 Bus*
Fully buffered, addressable in 4K blocks, Plugs right in most S-100 computers. 2 versions of bank select: bank byte or bank port.

Cat No.		
1601A	450ns kit	$285
1601B	200ns kit	$330
1602A	450ns a&t	$330
1602B	200ns a&t	$375
1603	bbd only	$27

CCS APPLE & S-100
PROTOTYPING BOARDS
Signals labeled on board.

Cat No.	Description	Price
1606	Apple Wirewrap	$21
1607	Apple soldertail	$21
1608	Apple etch	$18
1604	S-100 soldertail	$26
1605	S-100 wirewrap	$26
1609	S-100 etch	$23

CCS 7811A
APPLE II ARITHMETIC PROCESSOR
Add high powered math to your Apple! Increases math power by 10x! For number crucnhing, graphics.
Cat No. 1635 a&t $390

CCS GPIB
IEEE 488 BUS INTERFACE
Interface test equipment (equipped with 488 bus) to the Apple! Also interfaces the PET to the Apple.
Cat No. 2051 a&t $295

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Circle 162 on inquiry card.

What's New?

PUBLICATIONS

New COS/MOS Integrated Circuit Manual Issued by RCA



A new 168-page edition of the *RCA COS/MOS Integrated Circuits Manual*, CMS-272, is available for $5 from RCA Solid State Division, Rt 202, Somerville NJ 08876. This manual provides detailed information on the design, operation, and application of COS/MOS digital integrated circuits ranging from simple gates to highly complex large-scale integrated devices.

The manual begins with the basic principles of complementary symmetry MOS integrated circuits, and then describes the circuit elements from which the more complex COS/MOS integrated circuits are developed. It gives the features and characteristics of current RCA A-series and B-series types as well as device handling and operating considerations. Design examples and performance data are given for COS/MOS devices in a wide variety of circuit applications, such as, astable and monostable multivibrators, crystal oscillators for digital timekeeping, shift registers and counters, display drivers, and digital frequency synthesizers.

New material includes an introduction to microprocessors and memory interfacing, as well as guidelines to the design of custom large-scale integrated circuits. The information in this manual is presented in thirteen well-illustrated, easy-to-read text sections.

Circle 545 on inquiry card.

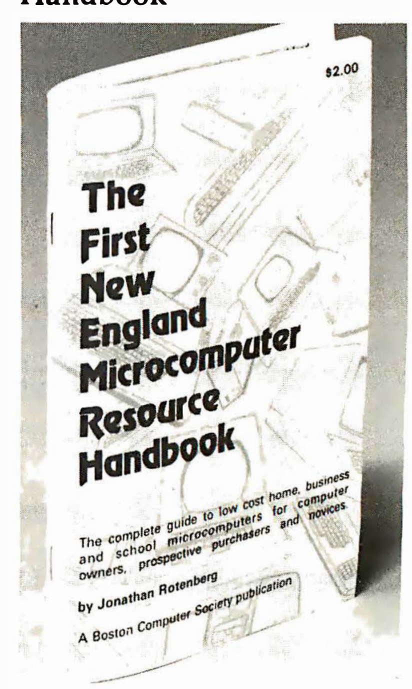
Management Guide to 100 Word Processors

This new report tells a manager which word processors are commonly used in different industries, which models are used in specific applications, who services the system after it is purchased, and which word processors are feasibly priced. In addition to charting this information for 100 models, the guide provides a directory of suppliers, which includes name, address, and phone number.

Word Processing Market Report is available for $15 from Alltech Publishing Co, 212 Cooper Ctr, N Park Dr and Browning Rd, Pennsauken NJ 08109.

Circle 549 on inquiry card.

The First New England Microcomputer Resource Handbook



This guide to microcomputers for novices, prospective purchasers and system owners contains sections on product comparisons, application software, buying tips, support devices, computer stores, introductory information, publications, user groups, consultants, books, repair companies and a glossary which defines buzz words in terms of real-life situations. The, 115-page book is available for $2 from New England computer stores or from The Boston Computer Society, 17 Chestnut St, Boston MA 02108.

Circle 550 on inquiry card.

Belais' Master Index to Computer Programs in BASIC

Source information and detailed reviews of 531 documented, ready-to-run programs in 72 fields covering home and business are included in this book. Updates and reprints also are listed. The book utilizes technical and layman's languages to describe the programs.

This 192-page paperback is available for $9.95 plus $1 shipping from Falcon Publishing, Dept G, 140 Riverside Ave, POB 688, Ben Lomond CA 95005.

Circle 546 on inquiry card.

PET Quick Reference Card

This card contains a complete summary of the Commodore PET BASIC language along with examples and definitions of every command and a table of the PET's graphic characters with their hexadecimal equivalents. Programmers will find a table of memory locations as well as information on the user port, PET sound, and the IEEE-488 interface bus.

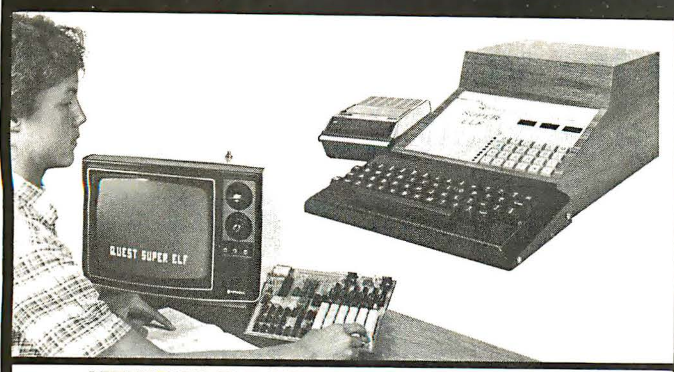
The price is $3.50. For more information, contact Leading Edge Computer Products, POB 3872, Torrance CA 90510.

Circle 547 on inquiry card.

Free Word Processing Supplies Guide

An 84-page illustrated *Guide to Word Processing Accessories and Supplies, 1979 Edition*, describing almost 1300 items for word and data processing installations, is available from American Word Processing Co, 18730 Oxnard St, Tarzana CA 91356. Included are many 5-inch and 8-inch disk storage systems, anti-static mats, video work stations, fireproof media safe, competitive brands of Diablo and Qume printer ribbons, various lines of durable plastic printwheels, thimbles, and ribbons for the NEC Spinwriter printers and more.

Circle 548 on inquiry card.



ATTENTION ELF OWNERS: QUEST SUPER BASIC

Quest, the leader in inexpensive 1802 systems announces another first. Quest is the first company worldwide to ship a full size *Basic* for 1802 systems. A complete function Super Basic by Ron Cenker including floating point capability with scientific notation (number range $\pm .17E^{38}$), 32 bit integer ±2 billion, Multi dim arrays, String arrays, String manipulation, Cassette I/O, Save and load, Basic, Data and machine language programs and over 75 Statements, Functions and Operators.

Easily adaptable on most 1802 systems. Requires 12K RAM minimum for Basic and user programs. Cassette version in stock now. ROM versions coming soon with exchange privilege allowing some credit for cassette version.

Super Basic on Cassette $40.00

Tom Pittman's 1802 Tiny Basic Source listing now available. Find out how Tom Pittman wrote Tiny Basic and how to get the most out of it. Never offered before. $19.00

S-100 Slot Expansion $9.95

Coming Soon: Assembler and Editor; Elf II Adapter Board. High resolution alpha/numerics with color graphics expandable up to 256 x 192 resolution for less than **$100.**

16K Dynam. RAM bd. expand. 32K; less than $150.

RCA Cosmac Super Elf Computer $106.95

Compare features before you decide to buy any other computer. There is no other computer on the market today that has all the desirable benefits of the **Super Elf** for so little money. The Super Elf is a small single board computer that does many **big** things. It is an excellent computer for training and for learning programming with its machine language and yet it is easily **expanded** with **additional memory, Full Basic, ASCII Keyboards, video character generation, etc.**

Before you buy another small computer, see if it includes the following features: ROM monitor; State and Mode displays; Single step; Optional address displays; Power Supply; Audio Amplifier and Speaker; Fully socketed for all IC's; Real cost of in warranty repairs; Full documentation.

The **Super Elf** includes **a ROM** monitor for program loading, editing and execution with **SINGLE STEP for program debugging** which is not included in others at the same price. With **SINGLE STEP** you can see the microprocessor chip operating with the **unique Quest** address and data bus displays **before, during** and **after** executing instructions. Also, CPU mode and instruction cycle are decoded and displayed on 8 LED indicators.

An RCA 1861 **video graphics** chip allows you to connect to your own TV with an inexpensive video modulator to do graphics and games. There is a **speaker system** included for writing your own music or using many music programs already written. The speaker amplifier may also be used to drive relays for control purposes.

A 24 key **HEX keyboard** includes 16 HEX keys plus **load, reset, run, wait, input, memory protect, monitor select** and **single step**. Large, on board displays provide output and optional **high** and **low address**. There is a 44 pin standard connector slot for PC cards and a 50 pin connector slot for the Quest Super Expansion Board. Power supply and sockets for **all** IC's are included in the price plus a detailed 127 pg. instruction manual which now includes over 40 pgs. of software info. including a series of lessons to help get you started and a music program and graphics target game.

Many schools and universities are using the Super Elf as a course of study. OEM's use it for training and research and development.

Remember, other computers only offer Super Elf features at additional cost or not at all. **Compare before you buy. Super Elf Kit $106.95, High address option $8.95, Low address option $9.95. Custom Cabinet** with drilled and labelled plexiglass front panel **$24.95.** Expansion Cabinet with room for 4 S-100 boards **$41.00. NiCad Battery Memory Saver Kit $6.95.** All kits and options also completely assembled and tested.

Questdata, a 12 page monthly software publication for 1802 computer users is available by subscription for $12.00 per year.

Tiny Basic Cassette **$10.00,** on ROM **$38.00,** original Elf kit board **$14.95. 1802 software;** Moews Video Graphics **$3.50.** Games and Music **$3.00,** Chip 8 Interpreter **$5.50.**

Super Expansion Board with Cassette Interface $89.95

This is truly an astounding value! This board has been designed to allow **you** to decide how you want it optioned. **The Super Expansion Board comes with 4K of low power RAM** fully addressable anywhere in 64K with built-in memory protect and **a cassette interface**. Provisions have been made for all other options on the same board and it fits neatly into the hardwood cabinet alongside the **Super Elf**. The board includes slots for up to 6K of **EPROM** (2708, 2758, 2716 or TI 2716) and is **fully socketed.** EPROM can be used for the monitor and Tiny Basic or other purposes.

A 1K Super ROM Monitor $19.95 is available as an on board option in 2708 EPROM which has been preprogrammed with a program loader/editor and error checking multi file cassette read/write software, (relocatible cassette file) another exclusive from Quest. It includes register save and readout, block move capability and video graphics driver with blinking cursor. Break points can be used with the register save feature to isolate program bugs quickly, then follow with single step. The Super Monitor is written with subroutines allowing users to take advantage of monitor functions simply by calling them up. Improvements and revisions are easily done with the monitor. If you have the **Super Expansion Board** and **Super Monitor** the monitor is up and running at the push of a button.

Other on board options include **Parallel Input and Output Ports** with **full handshake**. They allow easy connection of an ASCII keyboard to the input port. **RS 232 and 20 ma Current Loop** for teletype or other device are on board and if you need more memory there are two **S-100** slots for static RAM or video boards. Also a 1K Super Monitor version 2 with video driver for full capability display with Tiny Basic and a video interface board. **Parallel I/O Ports $9.85, RS 232 $4.50, TTY 20 ma I/F $1.95, S-100 $4.50. A 50 pin connector set** with ribbon cable is available at $12.50 for easy connection between the **Super Elf** and the **Super Expansion Board.**

Power Supply Kit for the complete system (see Multi-volt Power Supply below).

Multi-volt Computer Power Supply

8v 5 amp, ±18v .5 amp, 5v 1.5 amp, −5v .5 amp, 12v .5 amp, −12 option. ±5v, ±12v are regulated. Kit $29.95. Kit with punched frame $37.45, $4.00 shipping. Woodgrain case $10.00, $1.50 shipping.

60 Hz Crystal Time Base Kit $4.40

Converts digital clocks from AC line frequency to crystal time base. Outstanding accuracy. Kit includes: PC board, IC, crystal, resistors, capacitors and trimmer.

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7402N	.18
7404N	.19
7409N	.23
7410N	.18
7414N	.70
7420N	.18
7422N	.39
7430N	.20
7442N	.50
7445N	.69
7447N	.60
7448N	.69
7450N	.18
7474N	.35
7475N	.49
7485N	.88
7489N	1.85
7490N	.43
7492N	.43
7493N	.43
7495N	.69
74100N	.90
74107N	.35
74121N	.34
74123N	59
74125N	.45
74145N	.69
74150N	.95
74151N	.69
74154N	1.00
74157N	.69
74161N	.87
74162N	.87
74163N	.87
74174N	.96
74175N	.90
74190N	1.15
74192N	.87
74193N	.85
74221N	2.00
74298N	1.65
74365N	66
74366N	.66
74367N	.66

74LS00 TTL	
74LS00N	.35
74LS02N	.35
74LS04N	.35
74LS05N	.35
74LS08N	.35
74LS10N	.35
74LS13N	.55
74LS14N	1.10
74LS20N	.35
74LS22N	.35
74LS28N	.41
74LS30N	.35
74LS33N	.75
74LS38N	.55
74LS74N	1.25
74LS75N	1.00
74LS90N	.85
74LS93N	.70
74LS95N	1.10
74LS107N	.45
74LS112N	.45
74LS113N	.35
74LS132N	.89
74LS136N	.45
74LS151N	.85
74LS155N	.85
74LS157N	85
74LS162N	1.15
74LS163N	1.15
74LS174N	2.00
74LS190N	1.06
74LS221N	1.95
74LS258N	.67
74LS367N	1.35

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LM323K-5	5.95
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LM320K-15	1.50
LM320T-5	1.60
LM320T-8	1.60
LM320T-12	1.50
LM320T-15	1.60
LM324N	1.15
LM339N	1.55
LM340K-5	1.35
LM340K-8	1.35
LM340K-12	1.35
LM340K-15	1.35
LM340K-24	1.35
LM340T-5	1.25
LM340T-8	1.25
LM340T-12	1.25
LM340T-15	1.25
LM340T-18	1.25
LM340T-24	1.25
LM343H	4.50
LM350	7.50
LM370	1.15
LM377	3.00
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LM380N	1.00
LM381	1.60
LM382	1.60
LM703H	40
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LM723H/N	.50
LM733N	.67
LM741CH	.35
LM741N	.32
LM747H/N	.75
LM748N	.35
LM1303N	1.75
LM1304	1.10
LM1305	1.27
LM1307	2.00
LM1310	2.75
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CD4006	1.10
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CD4008	.28
CD4009	.45
CD4010	.45
CD4011	.28
CD4012	.28
CD4013	.39
CD4014	1.00
CD4015	1.00
CD4016	.45
CD4017	1.05
CD4018	.94
CD4019	.45
CD4020	1.02
CD4021	1.25
CD4022	1.10
CD4023	.28
CD4024	.75
CD4025	.28
CD4026	2.00
CD4027	.66
CD4028	.85
CD4029	1.02
CD4030	.45
CD4035	1.02
CD4040	1.02
CD4042	.85
CD4043	85
CD4044	.85
CD4046	1.67
CD4049	.45
CD4050	.49
CD4051	1.13
CD4060	1.42
CD4066	.71
CD4068	.40
CD4069	.40
CD4070	.50
CD4071	.28
CD4072	.28
CD4073	.28
CD4075	.28
CD4076	1.45
CD4078	.40
CD4081	.28
CD4082	.28
CD4116	.47
CD4490	5.50
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CD4508	4.25
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CD4511	.94
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21L02-1	1.18
21F02	1.25
2104A-4	4.95
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2732	115.00
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8748	75.00
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N82S123	3.50
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8	.15	22	.30
14	.14	24	.35
16	.16	28	.42
18	.27	36	.58
20	.29	40	.57

2 level 14 pin ww 20

WIRE WRAP LEVEL 3

PIN		PIN	
14	.32	24	.86
16	.33	28	1.00
18	57	40	1.23

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2 MHz	4.50
4 MHz	4.25
5 MHz	4.25
10 MHz	4.25
18 MHz	3.90
20 MHz	3.90
32 MHz	3.90
32768 MHz	4.00
1.8432 MHz	4.50
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2N222A	.27
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2N2904A	.20
2N2907A	.25
2N3053	.40
2N3638	.25
2N3643	.25
2N3904	.18
2N3906	.18
2N3055	.69
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RESISTORS ¼ watt 5%
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25 per type .025 — 350 piece pack
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DL704	CC	.300	1.25
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DL747/750	CA/CC	.600	1.95
DL750	CC	.600	1.95
FND359	CC	.357	.70
FND500/507	CC/CA	.500	1.35
FND503/510	CC/CA	.500	.90
FND800/807	CC/CA	.800	2.20
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DG8 Fluorescent			1.75
DG10 Fluorescent			1.75
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7520 Clairex photocells			.39
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MAN3640	CC	.30	1.10
MAN4610	CA	.40	1.20
MAN4640	CC	.40	1.20
MAN4710	CA	.40	.95
MAN4740	CC	.40	1.20
MAN6640	CC	.56	2.95
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Includes everything except case. 2-PC boards. 6-.50" LED Displays. 5314 clock chip, transformer, all components and full instructions. Orange displays also avail. **Same kit w/.80" displays.** Red only. **$21.95** Case **$11.75**

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ASCII KEYBOARD KIT — Assembled and Tested $95.95
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APPLE II I/O BOARD * KIT $49.00

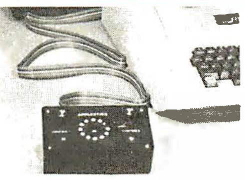
APPLE II I/O BOARD KIT — Plugs into Slot of Mother Board
• 1 8-Bit Parallel Output Port (expands to 3 Ports) • 1 Input Port • 15mA Output Current Sink or Source • Can be used for peripheral equipment such as printers, floppy discs, cassettes, paper tapes, etc. • 1 Free Software Listing for SWTP PR40 or IBM selectric. PRICE: 1 Input and 1 Output Port $49.00, 1 Input and 3 Outpot Ports $60.00. Dealer inquiries invited.

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Assembled and Tested $259.95 • Complete Unit with 4K Memory and Video Driver on Eprom assembled and tested $339.95. OPTIONAL: • Sockets $10.00 • 2K Memory $30.00 • 4K Memory $50.00 • Video Driver Eprom $20.00.

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MS-215 — 15 MHZ DUALTRACE PORTABLE SCOPE — $399.00
MS-15 15 MHZ SINGLE TRACE SCOPE — $299.00

SHIPPING $3.50 / California residents add 6% sales tax

ELECTRONICS WAREHOUSE Inc.
15820 Hawthorne Boulevard
Lawndale, CA 90260
(213) 370-5551





Circle 130 on inquiry card.

California Digital

Post Office Box 3097 B • Torrance, California 90503

FREE Paper Tiger

With Purchase of The INTEGRAL DATA 440

Your Choice, $200 Value

1) **Graphics Option Package**
2) **Interface for APPLE II**
3) **TRS-80 Printer Interface**

California Digital has resently researched the complete low cost printer market. It is our opinion that the IDS 440 Paper Tiger is, without doubt, the most versatile and offers the best value of any printer costing under $1,000.

This quality dot matrix printer incorporates such features as software selectable character size to allow print densities upto 132 characters per line. Full forms handling capabilities and tractor feed mechansim adjustable to 9.5". The Paper Tiger is engineered to accept either parallel or RS232 serial ASCII. 110/220V.50/60Hz.

***** $995.00 plus shipping *****

S-100 Mother Board

Quiet Buss

$29.95
8803-18
18 slot
IMSAI

The Quiet Buss from California Industrial is quality engineered. No short cuts have been taken to produce this mother board. Active termination circuitry prevents noise and crosstalk. Manufactured from extra heavy FR-4 epoxy glass

TELETYPE® MODEL 43

Even if we have to give them away, we're going to ship more 43's in 1979 than the aggregate of all our competitors.

Model 43AAA	TTL)		
EACH	3	10	25
$925.	875.	850.	825.

RS-232 Interface "K" Add $75.00 plus shipping

TELETYPE

Minidisk Drive for TRS-80

your choice **Lobo** or **Vista**

$388. Includes Interface Cable

FREE PLASTIC LIBRARY CASE

with purchase of each box of .... Verbatim mini-diskettes. $5 value.

$24.95 BOX of 10 **DISKETTES**

CONNECTORS

your choice
DB25P male plug & hood
or
DB25S female

$3.95



Qty.	fe.	male	hd.
10	3.45	2.45	1.15
25	3.15	2.25	1.05
100	2.85	1.90	.95
500	2.25	1.60	.85
1K	1.97	1.37	.73

Edge Connectors



GOLD 100 PIN IMSAI/ALTAIR

Imsai solder.125x.250	$3.95	3/$ 9 00
Imsai w/w.125centers	$4.95	3/$13.00
Altair soldertail.140row	$5.95	3/$15.00
SPECIALS		
22/44 Kim eyelet.156"	$1.95	3/$5.00
25/50 solder tab .156"	$1.09	3/$2.00
36/72 widepost w/w.156	$1.95	3/$5.00

SYSTEM X·10

It's not offen that California Digital ventures into the distribution of consumer products. but we have resently come accross a product that appear's so unique that we just had to add it to our product line. This is the System X-10 manufactured by the BSR turntable company. This space age system will remotely control any light or appliance in your home or office. Command signals are transmitted from the command console over your existing wiring. From your bed or easy chair you can control up to 16 different electrical devices inside and outside your home. Use the System X-10 to control your stereo, television or any light fixture on the premises.

The modular system is available in the following components:

Ultrasonic Master Control Console	$34.95
Battery Operated Ultrasonic Controller	19.95
Appliance Module, Lamp Module or Wall Switch	13.95

SPECiAL

APPLE II
16K MEMORY
COLOR • GRAPHICS • SOUND

$988 PLUS SHIPPING

Mfg.Sug. Retail.... $1195

TEN for $39, 50+ $3.65 — Scotch® BRAND

DISKETTES

8 inch Soft (IBM)
8 inch 32 sector
Mini Soft sec.
Mini 10 sector
Mini 16 sector

Certified Digital CASSETTES

Won't drop a BIT!

$5.50



CALIFORNIA INDUSTRIAL is an Authorized Dealer of Scotch Brand Data Products

Shugart Associates

SA800-R Floppy Disk Drive

The most cost effective way to store data processing information, when random recall is a prime factor. The SA800 is fully compatible with the IBM 3740 format. Write protect circuitry, low maintenance & Shugart quality.

$449.50

$85 KEYBOARD ASCII ENCODED



KEYTRONIC ASCII & ASCII complement.
*Ten key data pad
*Cursor controls
*Six user switches
*Alpha Lock
*Auto repeat
*Single 5 volt.
*Glass reed.

NEW

MEMORY

TRS-80 / APPLE II $65

16k memory (8) 4116's

Installation is simple. Anyone who has ever changed a spark plug should be able to up-grade his microcomputer.

How can California Digital offer these memory up-grade sets at 25% below our competition? Simple, we buy in volume, wholesale to dealers and sell the balance directly to owners of personal microsystems. These 16K dynamic memory circuits are factory prime and unconditionally guaranteed for one full year. NOW, before you change your mind, pick up the telephone and order your up-grade memory from California Digital. Add $3 for TRS80 jumpers.

STATIC	1-31	32-99	100-5C	-999	1K+
21L02 450nS.	1.19	.99	.95	.90	.85
21L02 250nS.	1.49	1.39	1.25	*	*
2114 1Kx4 450	5.95	5.50	5.25	4.75	4.50
2114 1Kx4 300	8.95	8.50	8.00	*	*
4044 4Kx1 450	5.95	5.50	5.25	*	*
4044 4Kx1 250	9.95	9.50	9.00	*	*
4045 1Kx4 450	8.95	8.50	8.00	*	*
4045 1Kx4 250	9.95	9.50	9.00	*	*
5257 low pow.	5.95	5.50	5.00	4.80	4.60

SPECIAL CIRCUITS

Z80A 4 MHz.	24.95	AY5-1013A UART	4.95
8080A CPU	9.95	Floppy Disc Controllers	
8085	22.50	WD 1771 single D.	39.95
8086 Intel 16 bits	85.00	WD 1781 Double D	65.00
TMS 9900 16 bits	49.95	WD 1791 D/D 3740	*



EPROMS		1-15	16-63	64+
1702A	2K	4.95	4.50	4.00
2708	8K	9.95	9.50	9.00
2716 5v	16K	39.95	35.00	*
2716 TI		24.88	20.00	*
2532		85.00	*	*

Buying a CRT Terminal? Hazeltine • Soroc • Lear Siegler

$850

Well if you really insist upon purchasing one of the above terminals, sure, we'll sell it to you. But when the keyboard starts to double bounce, the screen fades and the power supply just craps out don't call us, complain to the manufacturer.

The alternative, take a serious look at the ADDS Regent 25, we have, and concluded that this terminal offers, the best value in todays market. Through years of research the ADDS Company has evolved a low maintenance, extremely durable CRT terminal capable of withstanding an abusive 24 hour duty cycle. The Regent 25 features Intel 8085 microprocessor controlled circuitry along with the Cherry Switch long-life capacitance keyboard.

18 key cursor and numeric pad doubles to allow for user definable special functions. True descending lower case characters along with a fully addressable cursor makes the Regent 25 the ideal word processing terminal.

High-resolution screen is capable of displaying 96 upper and lower case ASCII characters and 32 control codes. This unique feature assist in the debugging of programs. The Regent 25 is switch selectable to display six European languages along with Katakana.

Clearly the Regent 25 is not your adverage terminal, but than, ADDS is not your adverage terminal company.

Regent® 25 from APPLIED DIGITAL DATA SYSTEMS

MINIATURE SWITCHES



your choice

	10	50	100	1k
$.98	$.88	.81	.73	.66

SPDT Miniature Toggles

7101 C&K	ON-NONE-ON
7107 jbt	ON-OFF(mnt.ON)
7108 CK	ON-(moment. ON)
Rocker JBT ———	DPDT
Rotary	3P-4-Pos.
Rotary	3P-6-Pos.
Push B (N.O.)	$.39ea. 4/$1

DIP Switch

	10	25	100	1K
$1.29 ea.	$1.19	1.09	.97	.83

specify 4, 7 or 8 pos.

SPST

$139.50 PORTABLE DATA ENTRY SYSTEM

These used data terminals were originally designed for chain store inventory control and order entry systems. The operator enters the inventory control number, merchandise on hand and the unit price. After all pertinent data has been entered into the recorder. the main warehouse is telephoned. the handset is placed in the acoustic coupler and all the recorded information is transmitted back to the master computer. With a little imagination and one of these portable entry systems, you should be able to exchange programs and computer information with associates across the country. All units were removed from service in working condition. Original cost $2,500.

Each system comes complete with:

- Portable Cassette Drive Unit
- Removable Entry Keyboard with LED Display
- Five Gould "D" NiCads
- Acoustical Coupler
- Battery Charger
- DB25 Cable
- Shoulder starp
- Full Documentation

DISCOUNT Wire Wrap Center

IC SOCKETS

pin	wire wrap ea.	25	50	low profile ea.	25	50
8	———			17¢	16	15
14	37¢	36	35	18	17	16
16	38	37	36	19	18	17
24	99	93	85	36	35	34
40	169	155	139	63	60	58

KYNAR WIRE WRAP — 50ft. $.98

500	1,000	11,000
$9.	$15.	$105.

Battery wire wrapping tool $34.95 **$29.95** BW630

OK HOBBY WRAP-30 wire wrap & strip tool **$5.45**

VISA



(213) 679-9001

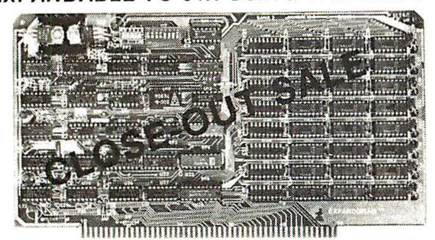
All merchandise sold by California Digital is premium grade. Sorry, no COD's. Orders are shipped the same day received. California residents add 6%. Foreign orders add 10%. Orders over $25, when accompanied by payment, are shipped at our expense. Otherwise, please add $2.

Circle 39 on inquiry card.

JADE Computer Products

*As **JADE** enters its fourth year, we would like to express our appreciation to all our friends and customers who have supported us through the years. We could not have grown from a ten-employee, half-million dollar company into a fifty-employee, eight-million dollar company without your continuing support. We at **JADE** thank **YOU** for being part of our family and wish you a joyous Holiday Season.*

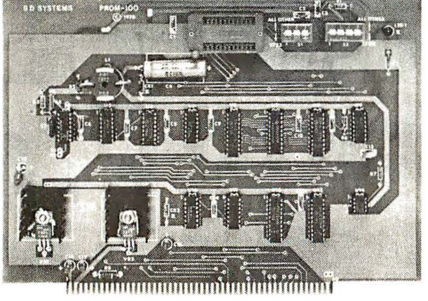
S D SYSTEMS
EXPANDORAM
EXPANDABLE TO 64K USING 4116 RAMS



Interfaces with most popular S-100 boards
Bank selectable; PHANTOM provision
Draws only 5 watts fully populated
Designed to work with Z-80, 8080, and 8085 systems
No wait states required
16K boundaries & protect via dip switches
Kits come with sockets for full 64K
Invisible refresh

MEM-16130K (16K KIT) **$199.00**
MEM-16130A (16K A&T) **$249.00**
MEM-32131K (32K KIT) **$265.00**
MEM-32131A (32K A&T) **$315.00**
MEM-48132K (48K KIT) **$339.00**
MEM-48132A (48K A&T) **$389.00**
MEM-64133K (64K KIT) **$394.00**
MEM-64133A (64K A&T) **$444.00**

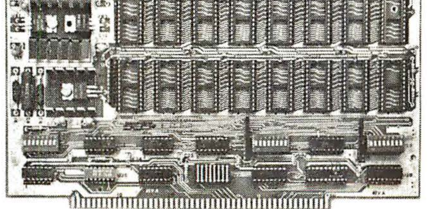
S D SYSTEMS
PROM-100
VERSATILE EPROM PROGRAMMER



S-100 bus compatible (note: board height 7")
Dip switch selects 2708, 2716, 2732, 2758, or 2516's
25 VDC programming pulse generated on board
Programming time only 100 seconds for 16K bits
Support-software listing provided in manual
Program and erasure verification
Software provides for reading of object file from CP/M and programming into EPROM

MEM-99520K (KIT) **$145.00**
MEM-99520A (A&T) **$215.00**

S D SYSTEMS
EXPANDOPROM
EXPANDABLE TO 32K USING 2716 EPROMS



S-100 bus compatible, uses 2708 or 2716 EPROMs
Dip switches allow selection of : each EPROM, 16K or 32K boundary, wait states

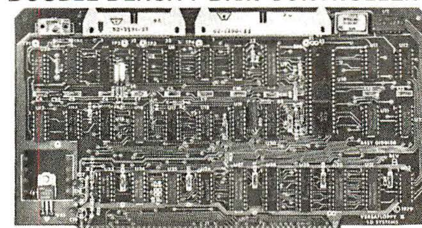
MEM-32220K (KIT) **$135.00**
MEM-32220A (A&T) **$199.00**

GET THE INSIDE TRACK
JADE DOUBLE-D
DOUBLE DENSITY DISK CONTROLLER

Read/write single or **double density,** 8" or 5¼" drives
On board Z-80 insures reliable operation
CP/M compatible in either single or double density
Density is software selectable
Up to 4 single or double sided, single or double density drives may be mixed on the same system
EIA level serial printer interface on board-up to 9600 baud (perfect for despooling operations)
All the hard work of disk access is done by the on board Z-80A and 2K memory, leaving your host CPU free for its normal duties
Uses IBM standard formats for proven reliability
THIS BOARD REALLY WORKS !!!!!!

IOD-1200K (DOUBLE-D KIT) **$285.00**
IOD-1200A (DOUBLE-D A&T) **$349.00**
IOD-1200D (MANUAL ONLY) **$15.00**

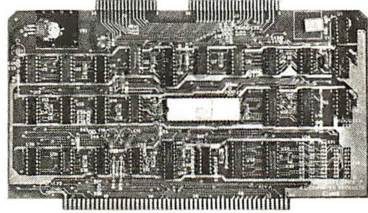
S D SYSTEMS
VERSAFLOPPY II
DOUBLE DENSITY DISK CONTROLLER



Single or double density floppy disk controller
985600 bytes on 8" double sided diskettes
259840 bytes on double sided 5¼" diskettes
S-100 bus (IEEE) standard compatible
IBM 3740 format in single density
8" and 5¼" drives controlled simultaneously
Operates with Z-80, 8080, and 8085 CPU's
Controls up to 4 drives
Vectored interrupt operation optional

IOD-1160K (KIT) **$305.00**
IOD-1169A (A&T) **$399.00**

S D SYSTEMS
VERSAFLOPPY
VERSATILE FLOPPY DISK CONTROLLER



IBM 3740 soft sectored format
S-100 Z-80 or 8080 compatible
Controls up to 4 single or double sided drives
Compatible with all popular disk drives
CP/M compatible
Listings for control software included

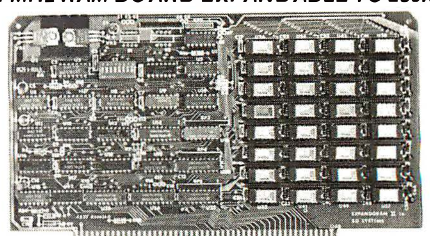
IOD-1150K (KIT) **$139.00**
IOD-1150A (A&T) **$229.00**

DECEMBER SPECIAL
JADE P/S I/O KIT
1 PARALLEL, 2 SERIAL I/O PORTS

One bi-directional parallel I/O port and two serial ports; one is RS232/TTL, the other is RS232/Kansas City Standard cassette interface

IOI-1040K (KIT) **$89.95**
IOI-1040A (A&T) **$159.95**
IOI-1040B (BARE BOARD) **$20.00**

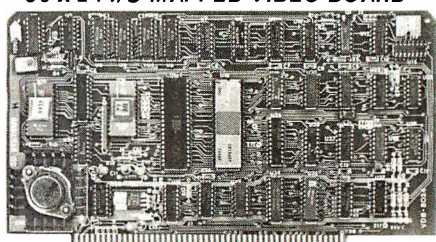
S D SYSTEMS
EXPANDORAM II
4 MHz RAM BOARD EXPANDABLE TO 256K



S-100 bus compatible, up to **4 MHz** operation
Expandable memory from 16K to 256K
Dip switch selectable boundaries
Page-mode allows up to 8 boards on the same bus
Invisible refresh; PHANTOM output disable
Designed to operate in Z-80 based systems

MEM-16631K (16K KIT) **$275.00**
MEM-16631A (16K A&T) **$325.00**
MEM-32632K (32K KIT) **$359.00**
MEM-32632A (32K A&T) **$410.00**
MEM-48632K (48K KIT) **$445.00**
MEM-48632A (48K A&T) **$495.00**
MEM-64632K (64K KIT) **$529.00**
MEM-64632A (64K A&T) **$579.00**

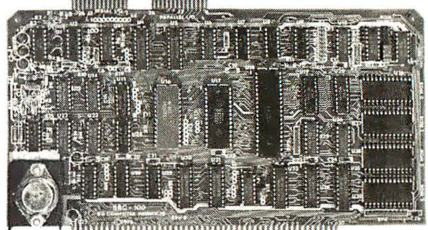
S D SYSTEMS
VDB-8024
80 X 24 I/O MAPPED VIDEO BOARD



80 character by 24 line display, 7 X 10 dot matrix
Composite or seperate TTL video outputs
On-board keyboard interface with power
On-board Z-80 and 2K RAM
Blink, underline, reverse, protect, up/down scroll
Upper/lower case characters, 32 special characters
Optional 128 user-programmable characters

IOV-1020K (KIT) **$295.00**
IOV-1020A (A&T) **$459.00**

S D SYSTEMS
SBC-100/200
2 OR 4 MHz SINGLE BOARD COMPUTER



S-100 bus compatible Z-80 CPU
1K of on-board RAM
4 EPROM sockets accomodates 2708, 2716, or 2732
One parallel and one serial I/O port
4-channel counter timer chip (Z-80 CTC)
Software programmable serial baud rates

CPC-30100K (2 MHz KIT) **$215.00**
CPC-30100A (2 MHz A&T) **$345.00**
CPC-30200K (4 MHz KIT) **$255.00**
CPC-30200A (4 MHz A&T) **$365.00**

SALE PRICES GOOD THRU JANUARY 5, 1980

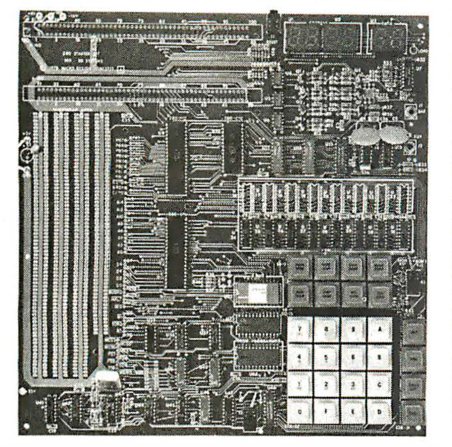
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PRICES *SLASHED* FOR DECEMBER !!!!

CALL TOLL-FREE AND SAVE

800-421-5809 CONTINENTAL U.S. 800-262-1710 INSIDE CALIFORNIA

S D SYSTEMS
Z-80 STARTER KIT
COMPLETE Z-80 MICROCOMPUTER



On-board keyboard, display, EPROM programmer, and cassette interface
On-board S-100 interface
Wire-wrap area and room for 2 S-100 connectors
Two 8-bit parallel I/O ports, 4-channel CTC, 5 programmable breakpoints
Examine and change memory, I/O ports, or register

CPS-30010K (KIT)	**$219.00**
CPS-30010A (A&T)	**$365.00**

CP/M 2.0

Digital Research has done it again! This new release of their industry standard disk operating system is bound to be an even bigger hit than the original version. All of the fundamental file-size restrictions of release 1 have been eliminated, while maintaining full compatibility with the earlier versions. This new release can be field-configured by the user for a single mini-disk up through a multiple drive hard-disk system with 128 megabyte capacity. Field configuration can be accomplished easily through use of the Macro Library (DISKDEF) provided with CP/M 2.0.

A powerful operating system for only ... $150.00

JADE'S NEW MOTHERBOARDS
THE ISO-BUS
WE'RE PROUD OF OUR MOTHER!

6-SLOT	
BARE BOARD	$24.95
KIT	$49.95
ASSEMBLED & TESTED	$59.95
12-SLOT	
BARE BOARD	$39.95
KIT	$89.95
ASSEMBLED & TESTED	$99.95
18-SLOT	
BARE BOARD	$59.95
KIT	$129.95
ASSEMBLED & TESTED	$149.95

SPECIAL PACKAGE PRICE
ROCKWELL AIM-65
THE HEAD-START IN MICROCOMPUTERS

KIM-1 compatible
On-board printer
Full ACSII keyboard

AIM-65 w/1K RAM..$375.00
AIM-65 w/4K RAM..$450.00
8K BASIC ROM..$100.00
POWER SUPPLY..$59.95
CASE for AIM-65..$49.95
4K Assembler/Editor..$80.00

Special Package Price $599.00
4K AIM-65, 8K BASIC ROM, Power Supply, and Case.

JADE
MEMORY EXPANSION KITS
FOR
TRS-80 APPLE EXIDY

Everything you need to add 16K of memory to your computer. Your kit comes neatly packaged with easy to follow instructions. In just minutes your computer is ready to tackle more advanced software.

$75.00

NEW REVISION C BOARD
THE BIG Z
Z-80 CPU BOARD WITH SERIAL I/O PORT

Features include ● S-100 Compatible available in 2MHz or 4MHz versions. ●On-board 2708, 2716, or 2532 EPROM can be addressed on any 1K, 2K or 4K boundary with power-on jump to EPROM. ● On-board EPROM may be used in SHADOW mode, allowing full 64K RAM to be used. ● Automatic MWRITE generation in front panel is not used. ●On-board USART for synchronous or asynchronous R232 operation (on-board baud rate generator). ●Reverse channel capability on USART allows use with buffered peripherals or devices with not-ready signal.

CPU-30200K (2 MHz KIT)	**$149.95**
CPU-30200A (2 MHz A&T)	**$199.95**
CPU-30201K (4 MHz KIT)	**$159.95**
CPU-30201A (4 MHz A&T)	**$209.95**

MICROPROCESSORS	
F8	$16.95
Z80 (2MHz)	$10.95
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CDP1802CD	$24.95
6502	$11.95
6800	$12.50
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8035	$24.00
8035-8	$24.00
8080-A	$10.00
8085	$23.00
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8080A SUPPORT DEVICES	
8212	$5.00
8214	$4.65
8216	$2.95
8224 (2MHz)	$4.30
8226	$2.75
8228	$6.40
8238	$6.40
8243	$8.00
8251	$7.50
8253	$20.00
8255	$6.40
8257	$19.95
8259	$19.95
8275	$69.95
8279	$17.70
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S2350	$10.95
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MC14411	$10.00

6800 PRODUCT	
6821P	$5.25
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6834P	$16.95
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6852P	$7.50
6860P	$9.25
6862P	$12.00
6875L	$7.30
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2513 Upper	$7.95
2513 Lower	$6.75
2513 Upper (5 volt)	9.75
2513 Lower (5 volt)	$13.00
MCM6571 up scan	$13.00
MCM6571A down scan	$10.95
PROMS	
1702A	
2708	$8.95
2716	$39.95
2716 (5v)	$39.95
2758 (5v)	$30.00
DYNAMIC RAMS	
4116/416D	8 for $74.95
2104/4096	$4.75
2107B-4	$3.95
TMS4027/4096	$4.75
STATIC RAMS	
21L02 (450ns)	$1.50
21L02 (250ns)	$1.75
2101-1	$2.95
2111-1	$3.25
2112-1	$2.95
2114L (450ns)	$5.75
2114L (300ns)	$5.95
TMS4044 (450ns)	$8.00
TMS4044 (300ns)	$9.95
410D (200ns)	$9.95
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Computer Products
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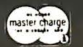
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800-421-5809 CONTINENTAL U.S.

WRITE FOR OUR FREE 1979 CATALOG
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TERMS OF SALE: Cash, checks, money orders, and credit cards accepted. **Minimum order $10.00.** California residents add 6% sales tax. Minimum shipping and handling charge $2.50. Prices are for U.S. and Canadian delivery only and are subject to change without notice. For export prices and information send for a ***JADE INTERNATIONAL CATALOG.***

master charge





INTEGRAL DATA SYSTEMS
THE PAPER TIGER
132 COLUMN DOT MATRIX PRINTER

Up to 198 CPS
1.75 to 9.5 inch adjustable tractor and friction feed.
Parallel and serial interface.
98 character ASCII set.
80 to 132 columns.
6 or 8 lines per inch.
Eight software selectable character sizes.
110, 300, 600, or 1200 baud.

PRM-33440	**$995.00**
PRM-33441 (with graphics & 2K buffer)	**$1195.00**

DISKETTE SPECIAL

5.25" SOFT, 10, OR 16 SECTOR
10 for **$29.95**
8" SOFT SECTOR IBM COMPATIBLE
10 for **$34.95**

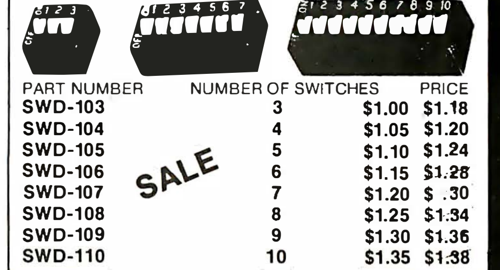
S-100 CONNECTOR SALE



100 PIN IMSAI TYPE SOLDER-TAIL CONNECTOR

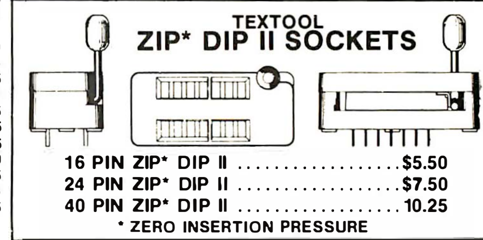
6** for **$15.00 ***12** for **$25.00***

SPST DIP SWITCHES



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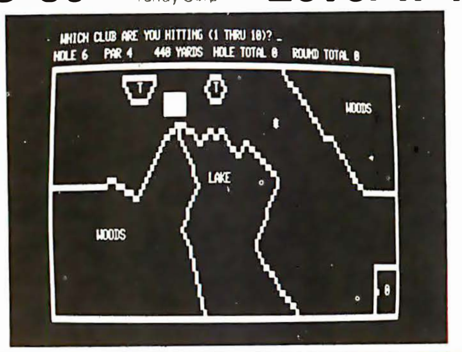
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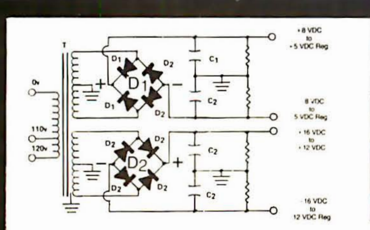
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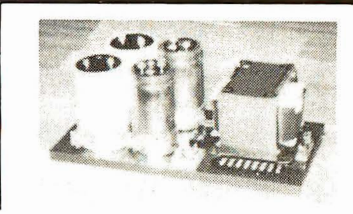
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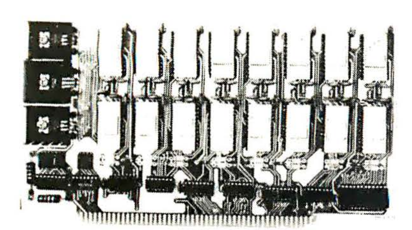
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$59.95 KIT

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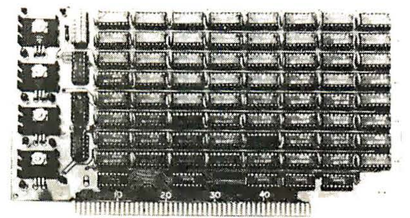
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(450 NS RAMS!)

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FOR 250NS ADD $10

FULLY STATIC, AT DYNAMIC PRICES

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We feel the 2114 will be the next industry standard RAM chip (like the 2102 was). This means price, availability, and quality will all be good! Next, the 2114 is FULLY STATIC! We feel this is the **ONLY** way to go on the S-100 Buss! We've all heard the HORROR stories about some Dynamic Ram Boards having trouble with DMA and FLOPPY DISC DRIVES. Who needs these kinds of problems? And finally, even among other 4K Static RAM's the 2114 stands out! Not all 4K static Rams are created equal! Some of the other 4K's have **clocked** chip enable lines and various timing windows **just as critical** as Dynamic RAM's. Some of our competitor's 16K boards use these "tricky" devices. But not us! The 2114 is the ONLY logical choice for a trouble-free, straightforward design.

KIT FEATURES:

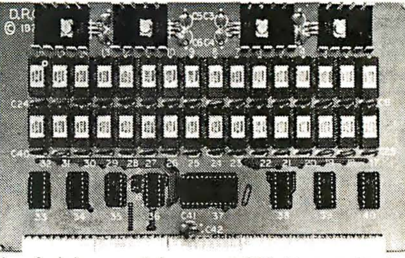
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FULLY STATIC AT DYNAMIC PRICES

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5. All Parts and Sockets included
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FOR SWTPC 6800 BUSS!

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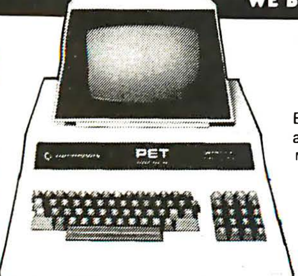
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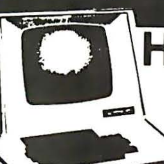
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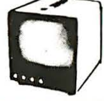
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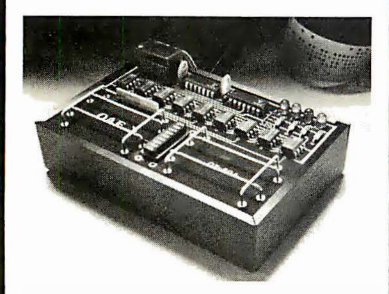
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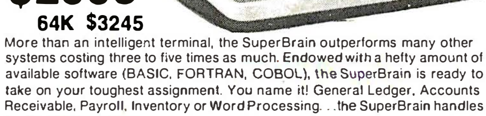
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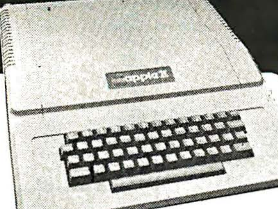
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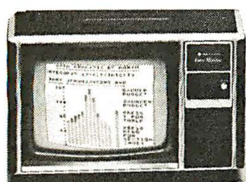
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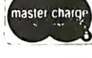
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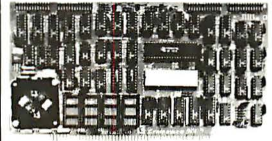
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74LS09	.35	74LS74	.45	74LS162	1.25
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SCC-W (Assembled) **$450.00**

Processor: 4MHz Z-80
Instruction Set: 158 instructions incl. the 78 instructions of the 8080.
ROM Capacity: 8K Bytes located from address 0000 to 1FFF.
ROM Type: Intel 2716 PROM or equivalent
RAM Capacity: 1K Bytes located from address 2000 to 23FF
RAM Type: 4045, Static

Serial I/O Ports:
I/O Levels: RS-232 or 20mA current loop
Baud Rates: 110 to 76,800 (software selectable)
Parallel Ports:
Input Port: 24 bits bidirectional
Output Port: 24 bits bidirectional
Input Load: One TTL equivalent
Output Drive: 20 TTL loads
Interval Timers:
Number of timers: 5

Timer range: 0-16.32 milliseconds (software sel.)
Timer resolution: 64 microseconds
Vectored Interrupts:
No. of restart locations (Z-80 mode): 65,536
General Information:
UART type: 5501 Bus: S-100
Power requirements: +8V at 1.4A; +18V at 70mA; -18V at 25mA
Operating environment: 0-55°C

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MM5369	2.95
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CT 7001	6.95

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MC1408L7	$4.95
MC1408L8	5.75
MC1439L	2.95
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MC3061P	3.50
MC4016(74416)	7.50
MC4024P	3.95
MC4040P	6.95
MC4044P	4.50

IC SOLDERTAIL — LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin LP	$.17	.16	.15	22 pin LP	$ .37	.36	.35
14 pin LP	.20	.19	.18	24 pin LP	.38	.37	.36
16 pin LP	.22	.21	.20	28 pin LP	.45	.44	.43
18 pin LP	.29	.28	.27	36 pin LP	.60	.59	.58
20 pin LP	.34	.32	.30	40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100		1-24	25-49	50-100
14 pin ST	$.27	.25	.24	28 pin ST	$ .99	.90	.81
16 pin ST	.30	.27	.25	36 pin ST	1.39	1.26	1.15
18 pin ST	.35	.32	.30	40 pin ST	1.59	1.45	1.30
24 pin ST	.49	.45	.42				

SOLDERTAIL STANDARD (GOLD)

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin SG	$.30	.27	.24	24 pin SG	$ .70	.63	.57
14 pin SG	.35	.32	.29	28 pin SG	1.10	1.00	.90
16 pin SG	.38	.35	.32	36 pin SG	1.65	1.40	1.26
18 pin SG	.52	.47	.43	40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100		1-24	25-49	50-100
8 pin WW	$.39	.38	.31	22 pin WW	$ .95	.85	.75
10 pin WW	.45	.41	.37	24 pin WW	1.05	.95	.85
14 pin WW	.39	.38	.37	28 pin WW	1.40	1.25	1.10
16 pin WW	.43	.42	.41	36 pin WW	1.59	1.45	1.30
18 pin WW	.75	.68	.62	40 pin WW	1.75	1.55	1.40
20 pin WW	.85	.79	.72				

1/4 WATT RESISTOR ASSORTMENTS — 5%

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ASST. 2	5 ea.	68 OHM 180 OHM	82 OHM 220 OHM	100 OHM 270 OHM	120 OHM 330 OHM	150 OHM 390 OHM	50 PCS	1.75
ASST. 3	5 ea.	470 OHM 1.2K	560 OHM 1.5K	680 OHM 1.8K	820 OHM 2.2K	1K 2.7K	50 PCS	1.75
ASST. 4	5 ea.	3.3K 8.2K	3.9K 10K	4.7K 12K	5.6K 15K	6.8K 18K	50 PCS	1.75
ASST. 5	5 ea.	22K 56K	27K 68K	33K 82K	39K 100K	47K 120K	50 PCS	1.75
ASST. 6	5 ea.	150K 390K	180K 470K	220K 560K	270K 680K	330K 820K	50 PCS	1.75
ASST. 7	5 ea.	1M 2.7M	1.2M 3.3M	1.5M 3.9M	1.8M 4.7M	2.2M 5.6M	50 PCS	1.75

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) **$9.95 ea.**

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TIL308	.27" red num. display w/integ. logic chip	10.95
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LITRONIX ISO-LIT 1
Photo Transistor Opto-Isolator
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SOUND GENERATOR
Generates Complex Sounds
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XR215	4.40			XR2556	3.20
XR320	1.55			XR2567	2.99
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XR555	.39	XR1800	3.20	XR4136	1.25
XR556	.99	XR2206	4.40	XR4151	3.95
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XR567CT	1.25	XR2208	5.20	XR4202	3.60
XR1310P	1.95	XR2209	1.75	XR4212	2.05
XR1468CN	3.85	XR2211	5.25	XR4558	.75
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XR1489	1.95	XR2240	3.45	XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
				1N4002	100 PIV	1 AMP	12/1.00
				1N4003	200 PIV	1 AMP	12/1.00
1N746	3.3	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N752	5.6	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N753	6.2	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N3600	50	200m	6/1.00
1N757	9.0	400m	4/1.00	1N4148	75	10m	15/1.00
1N759	12.0	400m	4/1.00	1N4154	35	10m	12/1.00
1N959	8.2	400m	4/1.00	1N4733	5.1	1w	28
1N965	15	400m	4/1.00	1N4734	5.6	1w	28
1N5232	5.6	500m	28	1N4735	6.2	1w	28
1N5234	6.2	500m	28	1N4736	6.8	1w	28
1N5235	6.8	500m	28	1N4738	8.2	1w	28
1N5236	7.5	500m	28	1N4742	12	1w	28
1N5242	12	500m	28	1N4744	15	1w	28
1N5245	15	500m	28	1N1183	50 PIV	35 AMP	1.60
1N456	25	40m	6/1.00	1N1184	100 PIV	35 AMP	1.70
1N458	150	7m	6/1.00	1N1185	150 PIV	35 AMP	1.70
1N485A	180	10m	5/1.00	1N1186	200 PIV	35 AMP	1.80
1N4001	50 PIV	1 AMP	12/1.00	1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A @ 400V	SCR(2N1849)	$1.95
C36M	35A @ 600V	SCR	1.95
2N2328	1.6A @ 300V	SCR	.50
MDA 980-1	12A @ 50V	FW BRIDGE REC.	1.95
MDA 980-3	12A @ 200V	FW BRIDGE REC.	1.95

TRANSISTORS

C106B1	.50			2N3904	4/1.00
MPSA05	.30	2N3055	.89	2N3905	4/1.00
MPSA06	5/1.00	MJE3055	1.00	2N3906	4/1.00
TIS97	6/1.00	2N3392	5/1.00	2N4013	3/1.00
TIS98	6/1.00	2N3398	5/1.00	2N4123	6/1.00
40409	1.75	PN3567	3/1.00	PN4249	4/1.00
40410	1.75	PN3568	4/1.00	PN4250	4/1.00
40673	1.75	PN3569	4/1.00	2N4400	4/1.00
2N918	4/1.00	MPS3638A	5/1.00	2N4401	4/1.00
2N2219A	2/1.00	MPS3702	5/1.00	2N4402	4/1.00
2N2221A	4/1.00	2N3704	5/1.00	2N4403	4/1.00
2N2222A	5/1.00	MPS3704	5/1.00	2N4409	5/1.00
PN2222 Plastic	7/1.00	2N3705	5/1.00	2N5086	4/1.00
2N2369A	4/1.00	MPS3705	5/1.00	2N5087	4/1.00
MPS2369	5/1.00	2N3706	5/1.00	2N5088	4/1.00
2N2484	4/1.00	MPS3706	5/1.00	2N5089	4/1.00
2N2906	4/1.00	2N3707	5/1.00	2N5129	5/1.00
2N2907	5/1.00	2N3711	5/1.00	PN5134	5/1.00
PN2907 Plastic	7/1.00	2N3724A	.65	PN5138	5/1.00
2N2925	5/1.00	2N3725A	1.00	2N5139	5/1.00
MJE2955	1.25	2N3772	2.25	2N5210	5/1.00
2N3053	2/1.00	2N3823	1.00	2N5449	3/1.00
		2N3903	5/1.00	2N5951	3/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100+		1-9	10-99	100+
10 pf	.05	.04	.03	.001µF	.05	.04	.035
22 pf	.05	.04	.03	.0047µF	.05	.04	.035
47 pf	.05	.04	.03	.01µF	.05	.04	.035
100 pf	.05	.04	.03	.022µF	.06	.05	.04
220 pf	.05	.04	.03	.047µF	.06	.05	.04
470 pf	.05	.04	.035	.1µF	.12	.09	.075

100 VOLT MYLAR FILM CAPACITORS

	1-9	10-99	100+		1-9	10-99	100+
.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (SOLID) CAPACITORS

	1-9	10-99	100+		1-9	10-99	100+
.1/35V	.28	.23	.17	1.5/35V	.30	.26	.21
.15/35V	.28	.23	.17	2.2/35V	.35	.31	.27
.22/35V	.28	.23	.17	3.3/25V	.35	.31	.27
.33/35V	.28	.23	.17	4.7/25V	.33	.28	.23
.47/35V	.28	.23	.17	6.8/25V	.49	.45	.35
.68/35V	.28	.23	.17	15/25V	.75	.68	.59
1.0/35V	.28	.23	.17	22/6V	.75	.60	.50

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead	1-9	10-99	100+	Radial Lead	1-9	10-99	100+
.47/50V	.15	.13	.10	.47/25V	.15	.13	.10
1.0/50V	.16	.14	.11	.47/50V	.16	.14	.11
3.3/50V	.14	.12	.09	1.0/16V	.15	.13	.10
4.7/25V	.15	.13	.10	1.0/25V	.16	.14	.11
10/25V	.15	.13	.10	1.0/50V	.16	.14	.11
10/50V	.16	.14	.12	4.7/16V	.15	.13	.10
22/25V	.17	.15	.12	4.7/25V	.15	.13	.10
22/50V	.24	.20	.18	4.7/50V	.16	.14	.11
47/25V	.19	.17	.15	10/16V	.14	.12	.09
47/50V	.25	.21	.19	10/25V	.15	.13	.10
100/25V	.24	.20	.18	10/50V	.16	.14	.12
100/50V	.35	.30	.28	47/50V	.24	.21	.19
220/25V	.32	.28	.25	100/16V	.19	.15	.14
220/50V	.45	.41	.38	100/25V	.24	.20	.18
470/25V	.33	.29	.27	100/50V	.35	.30	.28
1000/16V	.55	.50	.45	220/16V	.23	.17	.16
2200/16V	.70	.62	.55	470/25V	.31	.28	.26

Circle 200 on inquiry card.

ETCON AC/DC Voltage Tester



- High visibility voltage indicator 120, 208 to 240, 277, 440 to 600 VAC; 120, 240, 400, 600 VDC.
- Positive or negative DC pole identified by neon lamps.
- Provision for quick prod storage in case.
- Case serves as prod holder for one-hand operation. Self-extinguishing, high-impact case for long life.
- Continuous duty rated thru 480V.
- Dimensions: 4-9/16" x 2-1/16" x 7/8". Color: Orange.



VT200 .... $12.95

Custom Cables & Jumpers



DB 25 Series Cables

Part No.	Cable Length	Connectors	Price
DB25P-4-P	4 Ft.	2-DP25P	$15.95 ea.
DB25P-4-S	4 Ft.	1-DP25P/1-25S	$16.95 ea.
DB25S-4-S	4 ft.	2-DP25S	$17.95 ea.

Dip Jumpers

DJ14-1	1 ft.	1-14 Pin	$1.59 ea.
DJ16-1	1 ft.	1-16 Pin	1.79 ea.
DJ24-1	1 ft.	1-24 Pin	2.79 ea.
DJ14-1-14	1 ft.	2-14 Pin	2.79 ea.
DJ16-1-16	1 ft.	2-16 Pin	3.19 ea.
DJ24-1-24	1 ft.	2-24 Pin	4.95 ea.

For Custom Cables & Jumpers, See JAMECO 1979 Catalog for Pricing

25 PIN-D SUBMINIATURE CONNECTORS
(Meets RS232)

PART NO.	DESCRIPTION	PRICE
DB25P	PLUG (as pictured)	$2.95
DB25S	SOCKET	3.50
D851226-1	CABLE COVER for DB25P or DB25S	1.75
DB25P-B31	PLUG – Right Angle – P.C. Mount	4.95
DB25S-B31	SOCKET – Right Angle – P.C. Mount	5.25

Printed Circuit Connectors



.156 Spacing-Tin-Double Read-Out
Bifurcated Contacts
Fits .054 to .070 P.C. Boards

PART NO.	DESCRIPTION	PRICE
15/30 SE	15/30 Contacts – solder eyelet	$1.95
18/36 SE	18/36 Contacts – solder eyelet	2.49
22/44 SE	22/44 Contacts – solder eyelet	2.95
22/44 WW	22/44 Contacts – wire wrap	3.95
50/100 WW	50/100 Contacts – wire wrap (R681-1). (.125 Spacing)	6.95

Jumbo 6-Digit Clock Kit

- Four .630"ht. and two .300"ht. common anode displays
- Uses MM5314 clock chip
- Switches for hours, minutes and hold functions
- Hours easily viewable to 30 feet
- Simulated walnut case
- 115VAC operation
- 12 or 24 hour operation
- Includes all components, case and wall transformer
- Size: 6¾ x 3⅛ x 1¾

JE747 .... $29.95



- Bright .300 ht. comm. cathode display
- Uses MM5314 clock chip
- Switches for hours, minutes and hold modes
- Hrs. easily viewable to 20 ft.
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hr. operation
- Incl. all components, case & wall transformer
- Size: 6¾" x 3-1/8" x 1¾"

JE701

6-Digit Clock Kit $19.95

Micro-Miniature Joystick



- 2 each 100K pots (Linear Taper)
- Printed Circuit Board Mount
- Size: 1" x 1-3/16" x 1-3/16"

Micro-Miniature Joystick $4.95

Digital Stopwatch Kit

- Use Intersil 7205 Chip
- Plated thru double-sided P.C. Board
- LED display (red)
- Times to 59 min. 59.59 sec. with auto reset
- Quartz crystal controlled
- Three stopwatches in one: single event, split (cummulative) & taylor (sequential timing)
- Uses 3 penlite batteries
- Size: 4.5" x 2.15" x .90"

JE900 $39.95

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES			
8080A	CPU		$ 7.95
8212	8-Bit Input/Output		3.25
8214	Priority Interrupt Control		5.95
8216	Bi-Directional Bus Driver		3.49
8224	Clock Generator/Driver		3.95
8226	Bus Driver		3.49
8228	System Controller/Bus Driver		4.95
8238	System Controller		5.95
8251	Prog. Comm. 1/0 (USART)		7.95
8253	Prog. Interval Timer		14.95
8255	Prog. Periph. 1/0 (PPI)		9.95
8257	Prog. DMA Control		19.95
8259	Prog. Interrupt Control		19.95
6800/6800 SUPPORTOEVICES			
MC6800	MPU		$14.95
MC6802CP	MPU with Clock and Ram		24.95
MC6810APi	128X8 Static Ram		5.95
MC6821	Periph. Inter. Adapt (MC6820)		7.49
MC6828	Priority Interrupt Controller		12.95
MC6830L8	1024X8 Bit ROM (MC68A30-6)		14.95
MC6850	Asynchronous Comm. Adapter		7.95
MC6852	Synchronous Serial Data Adapt.		9.95
MC6860	0-600 bps Digital MODEM		12.95
MC6862	2400bps Modulator		14.95
MC6880A	Quad 3-State Bus. Trans. (MC8T26)		2.25
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Z80(780C)	CPU		$14.95
Z80A(780-1)	CPU		16.95
CDP1602	CPU		19.95
2650	MPU		19.95
6502	CPU		11.95
8035	8-Bit MPU w/clock, RAM, 1/0 lines		19.95
P8085	CPU		19.95
TMS9900JL	16-Bit MPU w/hardware, multiply & divide		49.95
SHIFT REGISTERS			
MM500H	Dual 25 Bit Dynamic		$.50
MM503H	Dual 50 Bit Dynamic		.50
MM504H	Dual 16 Bit Static		.50
MM506H	Dual 100 Bit Static		.50
MM510H	Dual 64 Bit Accumulator		.50
MM5016H	500/512 Bit Dynamic		.69
2504T	1024 Dynamic		3.95
2518	Hex 32 Bit Static		4.95
2522	Dual 132 Bit Static		2.95
2524	512 Static		.99
2525	1024 Dynamic		2.95
2527	Dual 256Bit Static		2.95
2528	Dual250 Static		4.00
2529	Dual 240 Bit Static		4.00
2532	Quad 80 Bit Static		2.95
3341	Fifo		6.95
74LS670	4X4 Register File (TriState)		2.49
UART'S			
A-Y-5-1013	30K BAUD		5.95
MICROPROCESSOR MANUALS			
M-Z80	User Manual		$7.50
M-CDP1802	User Manual		7.50
M-2650	User Manual		5.00
ROM'S			
2513(2140)	Character Generator(upper case)		$9.95
2513(3021)	Character Generator(lower case)		9.95
2516	Character Generator		10.95
MM5230N	2048-Bit Read Only Memory		1.95
RAM'S			
1101	256X1	Static	$1.49
1103	1024X1	Dynamic	.99
2101(8101)	256X4	Static	3.95
2102	1024X1	Static	1.75
21L02	1024X1	Static	1.95
2111(8111)	256X4	Static	3.95
2112	256X4	Static MOS	4.95
2114	1024X4	Static 450ns	7.95
2114L	1024X4	Static 450ns low power	10.95
2114-3	1024X4	Static 300ns	10.95
2114L-3	1024X4	Static 300ns low power	11.95
5101	256X4	Static	7.95
5280/2107	4096X1	Dynamic	4.95
7469	16X4	Static	1.75
74S200	256X1	Static Tristate	4.95
93421	256X1	Static	2.95
UPD414 (MK4027)	4K	Dynamic 16 pin	4.95
UPD416 (MK4116)	16K	Dynamic 16 pin 250ns	9.95
TMS4044-45NL	4K	Static	14.95
TMS4045	1024X4	Static	14.95
2117	16,384X1	Dynamic 350ns (house marked)	9.95
MM5262	2KX1	Dynamic	4/1.00
PROM'S			
1702A	2048	FAMOS	$5.95
2716INTEL	16K*	EPROM	59.95
TMS2516 (2716)	16K*	EPROM	49.95
	*Requires single +5V power supply		
TMS2532	4KX8	EPROM	89.95
2708	8K	EPROM	10.95
2716T.1	16K**	EPROM	29.95
	**Requires 3 voltages, —5V, +5V, +12V		
5203	2048	FAMOS	14.95
6301-1(7611)	1024	Tristate Bipolar	3.49
6330-1(7602)	256	Open C Bipolar	2.95
82S23	32X8	Open Collector	3.95
82S115	4096	Bipolar	19.95
82S123	32X8	Tristate	3.95
74186	512	TTL Open Collector	9.95
74188	256	TTL Open Collector	3.95
74S287	1024	Static	2.95

JE600 HEXADECIMAL ENCODER KIT



FEATURES:
- Full 8 bit latched output for microprocessor use
- 3 User Define keys with one being bistable operation
- Debounce circuit provided for all 19 keys
- LED readout to verify entries
- Easy interfacing with standard 16 pin 1C connector
- Only +5VDC required for operations

FULL 8 BIT LATCHED OUTPUT—19 KEYBOARD

The JE600 Encoder Keyboard provides two separate hexadecimal digits produced from sequential key entries to allow direct programming for 8 bit microprocessor or 8 bit memory circuits. Three (3) additional keys are provided for user operations with one having a bistable output available. The outputs are latched and monitored with LED readouts. Also included is a key entry strobe.

JE600 .... $59.95
Hexadecimal Keypad only $14.95

DIGITAL THERMOMETER KIT



- Dual sensors—switching control for in-door/outdoor or dual monitoring
- Continuous LED .8" ht. display
- Range: -40°F to 199°F / -40°C to 100°C
- Accuracy: ±1° nominal
- Set for Fahrenheit or Celsius reading
- Sim. walnut case - AC wall adapter incl.
- Size: 3-1/4"H x 6-5/8"W x 1-3/8"D

JE300 .... $39.95

62-Key ASCII Encoder Keyboard Kit



The JE610 62-Key ASCII Encoder Keyboard Kit can be interfaced into most any computer system. The JE610 Kit comes complete with an industrial grade keyboard switch assembly (62 keys), IC's, sockets, connector, electronic components and a double-sided printed wiring board. The keyboard assembly requires +5V @ 150mA and −12V @ 10mA for operation.

FEATURES:
- 60 Keys generate the full 128 characters, upper and lower case ASCII set
- Fully buffered
- 2 user-define keys provided for custom applications
- Caps lock for upper case only alpha characters
- Utilizes a 2376 (40 pin) encoder read only memory chip
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Easy interfacing with a 16-pin dip or 18-pin edge connector

JE610 ..... $79.95
62-Key Keyboard only . . $34.95

REGULATED POWER SUPPLY

NEW

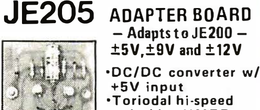
JE200 5V-1 AMP POWER SUPPLY



- Uses LM309K
- Heat sink provided
- PC Board construction
- Provides a solid 1 amp @ 5 volts
- Can supply up to ±5V, ±9V and ±12V with JE205 Adapter
- Includes components, hardware & instructions
- Size: 3½"x5"x2"H

JE200 $14.95

JE205 ADAPTER BOARD
– Adapts to JE200 –
±5V, ±9V and ±12V



- DC/DC converter w/ +5V input
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- Short circ. protection
- PC Brd. construction
- Piggy-back to JE200 board
- Size: 3½"x2"x9/16"h

JE205 $12.95

$10.00 Min. Order – U.S. Funds Only
Calif. Residents Add 6% Sales Tax
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1980 Catalog Available — Send 41¢ stamp

FREE 1980 CATALOG



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The Incredible "Pennywhistle 103"



$139.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method	Frequency-Shift Keying, full-duplex (half-duplex selectable).
Maximum Data Rate	300 Baud.
Data Format	Asynchronous Serial (return to mark level required between each character).
Receive Channel Frequencies	2025 Hz for space; 2225 Hz for mark.
Transmit Channel Frequencies	Switch selectable: Low (normal) = 1070 space, 1270 mark; High = 025 space, 2225 mark.
Receive Sensitivity	−46 dbm accoustically coupled.
Transmit Level	−15 dbm nominal. Adjustable from −6 dbm to −20 dbm.
Receive Frequency Tolerance	Frequency reference automatically adjusts to allow for operation between 1800 Hz and 2400Hz.
Digital Data Interface	EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar).
Power Requirements	120 VAC, single phase, 10 Watts.
Physical	All components mount on a single 5" by 9" printed circuit board. All components included.

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

TRS-80 16K Conversion Kit

Expand your 4K TRS-80 System to 16K.
Kit comes complete with:
- 8 each UPD416-1 (16K Dynamic Rams) 250NS
- Documentation for conversion

TRS-16K $75.00





JUST WRAP™

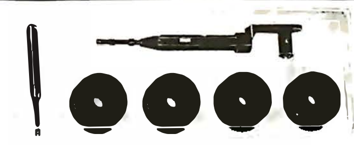
- 30 AWG wire
- Daisy chain or point-to-point
- No stripping or slitting required—just wrap
- .025" square posts
- Built-in cut off
- Includes 50 ft. wire

Part No.	Wire Color	Price
JW-1-B	Blue	$14.95
JW-1-W	White	14.95
JW-1-Y	Yellow	14.95
JW-1-R	Red	14.95

JUST WRAP™ Replacement Wire

Part No.	Color		Price
R-JW-B	Blue	50 ft. roll	$2.98
R-JW-W	White	50 ft. roll	2.98
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JUST WRAP™ Unwrap Tool $3.49



JUST WRAP™ Kit

- 50 ft. ea.: blue, white, red, yellow wire
- JUST WRAP Tool
- Unwrapping Tool

JWK-6 .... $24.95

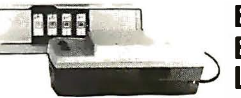


Vacuum Vise

Vacuum-based light-duty vise for small components and assemblies. ABS construction. 1½" jaws, 1¼" travel. Can be permanently installed.

VV-1 .... $3.49

EPROM Erasing Lamp



- Erases 2708, 2716, 1702A, 5203Q, 5204Q, etc.
- Erases up to 4 chips within 20 minutes.
- Maintains constant exposure distance of one inch
- Special conductive foam liner eliminates static build-up
- Built-in safety lock to prevent UV exposure
- Compact — only 7-5/8" x 2-7/8" x 2"
- Complete with holding tray for 4 chips

UVS-11E $69.95

IDEAL FOR TRS 80 — CASSETTE CONTROLLER

"Plug/Jack interface to any computer system requiring remote control of cassette functions"

The CC100 controls cassette motor functions, monitors tape location with its internal speaker and requires no power. Eliminates the plugging and unplugging of cables during computer loading operation from cassette.



#CC-100 $29.50

Circle 200 on inquiry card.

FLOPPY SYSTEMS



8" Siemens FDD120-8 All Siemens options included in this drive may be configured hard or soft and single or double density. We find this to be an extremely reliable drive. $399.00



5¼" BASF Magical Miniature Mini drive only 2/3 the size of others is reliable and durable and quickly gaining in popularity with our customers. Single or dual density fast access times $274.00

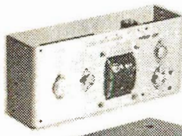


Tarbell Controller may be re-configured to control 5¼" drives and includes short cable for one drive. KIT $179.00, ASM $265, but only $219 with purch. of 2 drives.



Cable Kits For 8" Drives with 10' 50 cond. cable and connectors. Also power cable and connectors. Flat cable assem if you wish. For one drive 27.50, two 33.95, three 38.95

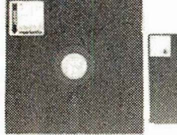
Cable Kits for 5¼" Drives as above, but 34 cond. For one drive **24.95**, two **29.95.**



"Power One" Model CP206 Power Supply adequate for at least two drives. 2.8A/24V 2.5A/5V, 0.5A/-5V beautiful quality. $99.00



CABINETS for FDD120 and 801R drives, or CP206 supply. Matte finish in mar resistant black epoxy paint and stacking design 29.95

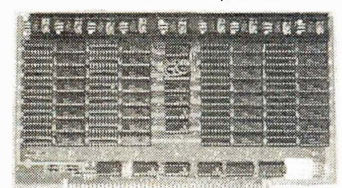




DISKETTES (3M, MRX, BASF, Georgia Magnetics, & Victor Borge)
8" $39.95/10
5¼" $29.95/10

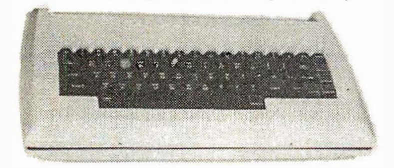
32K / 16K Static RAM, 4MHz.

(Showing Amazing Similarity to Tarbell's unit)
(16K Shown in photo)

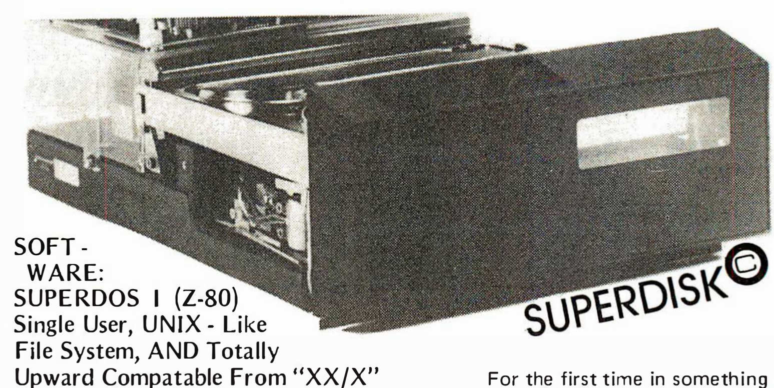


32K - $549.00 16K - $349.00

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CHERRY "PRO" Keyboard $119.00
Streamlined Custom Enclosure $34.95
BOTH ONLY $124.95 !!!!!!!!



10MBy DRIVE $3300

S-100 DMA CONTROL $495

POWER UNIT $395.00

SOFT-WARE:
SUPERDOS I (Z-80)
Single User, UNIX - Like File System, AND Totally Upward Compatable From "XX/X"
(What did you say, Digital Research??)

PS: SUPERDOS -I runs on the TRS-80, and can transform it from a toy computer to a real business machine !!!

For the first time in something like 10 years, a new STANDARD in removable media has evolved. Selected by Datapoint, and others who have not yet announced, this drive is beautifully simple and easy, if not trivial to maintain. 920kBy/sec. transfer rate, 3600 RPM 39 lbs and only 125 Watts.

Daisy Wheel Printers

Qume Sprint 3\45

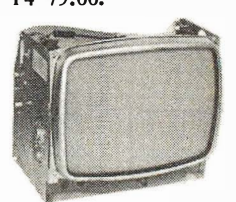
PRINTER (factory warr.) $1199.00
POWER SUPPLY (Boschert) $349.00
(shown mounted on rear of printer)
COMBINATION SPECIAL $1499.00

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POB 6721, Stanford, CA 94305
415-321-5601 800-227-8266
Telex: 345567 (Electrolab Pla)
Visa MC Am. Exp.

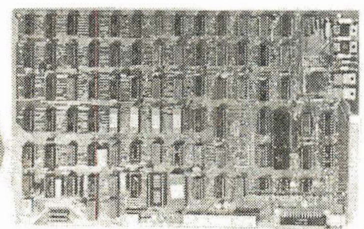
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Used 12" Sylvania monitors. Composite Video, 15 MHz, 120VAC. Rebuilt with NEW P39 anti-glare tube $119.00 New P4, 109.00, used P4 79.00.

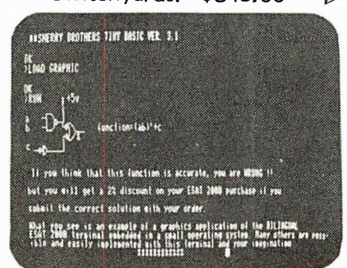


"OEM STYLE" as above, will fit any case. (Both versions serviced by qualified tech). Identical to above but subtract $12.00



ESAT 200B

BI-LINGUAL 80x24 COMMUNICATING TERMINAL
Scrolling, full cursor, bell, 8x8 matrix, 110 - 19,200 baud, Dual Font Applications. Arabic & Hebrew, Multilingual Data Entry Forms Drawing, Music, & Switchyards. $349.00



New!

Doppler Motion Sensor Intrusion Detector

Extremely effective microwave motion detector for detecting unwanted visitors. Ignores mice and other non-larcenous creatures. Operates on 12VDC or from small transformer supplied. Output is relay closure for alarm control interface, or to switch on lights annunciators. Will operate THROUGH door of closet or thin wall. Best application seems to be to turn on outside lights to help invited guests, and to intimidate unwanted ones. $159.00
Water Repellent Cover $24.95

SOCKET SPECIAL

BURNDY
"Won't Let Go"
Low Profile
Solder Tail
1 CENT/ Pin !! (0.75/1000's)
8 14 16 18 20 22 24 28 40

Circle 115 on inquiry card.

CP/M* Source Code -- FREE! *when you purchase* **"OS-1"**

Electrolabs' new operating system for the Z-80 designed to have exactly the appearance of UNIX, including virtual I/O, "set TTY", a tree and a shell, filters and pipes PLUS total compatability with CP/M software!**

OS-1© FEATURES

(Because OS-1 is truly a comprehensive "OS", and not merely a file handling "DOS", we have changed the name from "Superdos" to "OS-1")

VIRTUAL I/O - copy with a single command between floppy and hard disk, or from TTY to printer to tape to disk... etc., etc. No messy I/O routines to write, & no awkward transfers.
SECURITY - 9 modes of file protection, user and login protection.
MULTI-USER - up to 256 passwords. (non-simultaneous users)
16MBy FILE SIZE - but no limit to no. of directories per device, thus allowing EASY implementation of gigantic storage devices.
"SET TTY" - for printer or crt: tabs, page width, buffer, cursor, UC/LC, fonts, formfeed, arbitrary control characters etc., etc.
"LOGIN" - automatically executes user selected programs and "set TTY".
OCCUPIES 12KBy - only 50% larger than CP/M, but 500% more features.
CP/M & CDOS COMPATABLE - your library is guaranteed to run!

*(Naturally, we are not giving away the version of CP/M written by Digital Research, Please pardon our pun, but they might object. What we ARE giving you is a greatly enhanced version of CP/M which resides on OS-1, and allows the user of OS-1 to run any and all of his programs, packages or system utilities which are already running on CP/M. We give you the source code at no charge so that you may modify any part of the CP/M to suit your own system requirements. At no charge, you also receive the enhancement allowing 4MBy files instead of 256K.)

OS-1 (with debugger, linker and screen oriented editor	$199.00
Update service, per year	29.00
Symbolic Debugger	150.00
MACRO-Assembler (Creates relocatable code)	150.00
"C" Compiler	660.00
FORTRAN Compiler	100.00
BASIC Compiler (very fast)	150.00

A NEW System CONCEPT!!

BRAND NEW POWER!!
BRAND NEW OPERATING SYSTEM!!
UN-INTERRUPTABLE POWER CAPABILITY!!
DON'T LOSE YOUR DATA!!

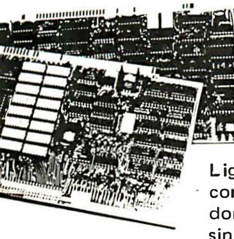
FEATURING: Expandability — hardware and OS expand — up to 16 users. Double density — (it works!!!) UNIX like operating system (OS-1). Supports all CP/M utilities and programs. Time sharing capability. Turnkey software included.

BUSINESS DATA WORK SAVER©!!!
Standard features: Enclosure, 10 slot backplane, Z-80 CPU, 32K RAM, I/O and controllers, Bantam terminal, Paper Tiger Printer, OS-1, Two floppies (8" or 5¼"). Basic compiler with application programs for accounts payable, accounts receivable, general ledger and payroll **$6495.00**

WORD SAVER©!!!
MULTI-USER
UP TO EIGHT STATION WORD PROCESSING
Standard features: Enclosure, 10 slot backplane, Z-80 CPU, 48K RAM, Daisy Wheel Printer, ESAT Terminal with two fonts (Arabic, Hebrew, Cyrillic, Greek, Catakana, any custom font for $50.00) Three floppies: (8" or 5¼") OS-1. Word processor package with additional memory which is expandable up to eight users (each extra terminal $900.00) **$8695.00**

ELECTROLABS
POB 6721 Stanford, CA 94305
415-321-5601 800-227-8266
Telex: 345567 (Electrolab Pla)

OPTIONS: 10 MBy hard disk (available now!!!) Extra memory, graphics, etc. Call or write for further details. This is the most advanced microcomputer system available at this time.



Graphics

High Resolution 480 x 512
for B&W and Color Imaging and Graphics

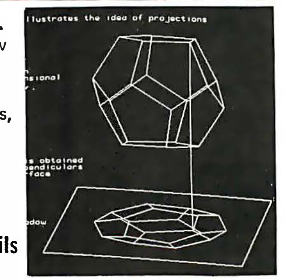
Light pen, A-D, D-A, TV synchro (needs no time base correction or adjustment with anything between random interface & NTSC commercial standard). T.V. single frame grabber ("snapshot"). Up to 1 Byte of attributions per pixel.

LSI-100 & S-100 applied to:
Graphic Presentation — such as computer generated animation & other graphic displays up to 256 colors & up to 256 b&w gray scales. **Image Analysis** — using built-in FRAME GRABBER, for medical image enhancement, contour analysis, & pattern recognition. **Commercial TV Tilting & Advertising** — using synchronization capability. **Interactive graphics** — using light pen accessory.

BASIC CONFIGURATION —
LSI-11 $1995. S-100 $1265.
For TRS-80/Exidy Add $595.00
Includes: Data Board - 32K (480 x 512 x 1 pixel) D-A 16 level video generator. Video Synchronization Circuitry. Address Control & Timing Board.

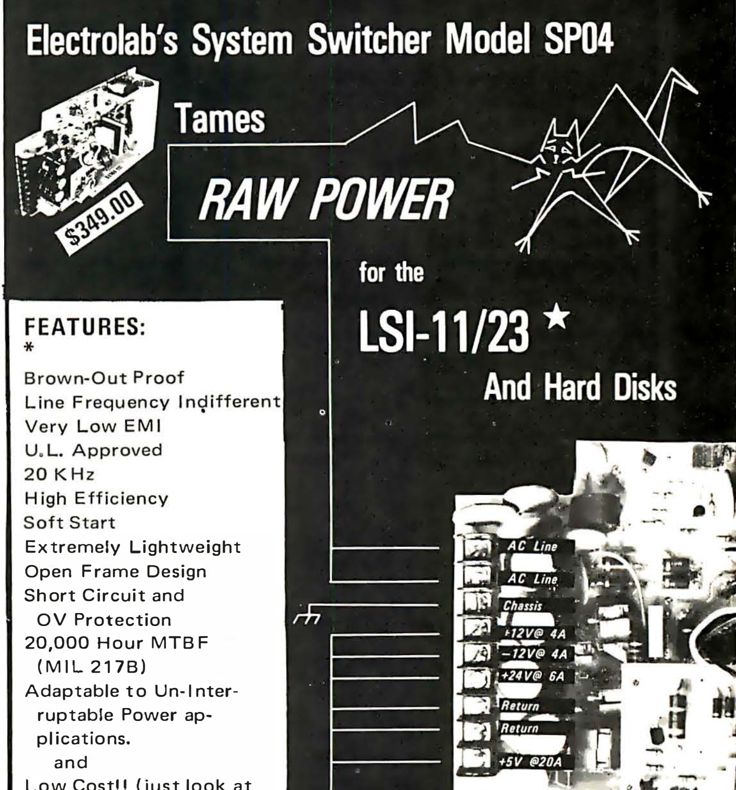
FEATURES — High speed. DMA or 2KBy window memory mapped interface. Full NTSC commercial color capability. Low power consumption. Excellent Software

Options — Accessories — Software
Options include: light pen, auxilliary outputs, text mode, memory and much more. Accessories include: b&w and color cameras and monitors. Software: "Plot" 2D or 3D, "Tilting", "Contour", "Image Enhancement", "Vector Curve Generation".



Call for price and details

*CPM and **UNIX trademarks of Digital Research and Western Electric respectively.



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DUMP-IN BASIC LEV2	$5.00
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SAVE TIME: Access the calls, keystrokes, and JSR's to those APPLE sub-routines that you know are there.
PLUS: Screen memory lay-out, Op-code Table, Character Table, Schematic of transfer operations, and **MUCH MORE.**
To Order: Send check for $1.95 and stamped, self-addressed envelope to:
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SPRINT 68 MICROCOMPUTER

CONTROL COMPUTER DEVELOPMENT SYSTEM

6800 MPU, serial I/O, 48K RAM, dual 8" drives, WIZRD multitasking DOS, Editor, Assembler, 12K BASIC all for $3995.

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TEACHERS!

THE ELECTRONIC ROLLBOOK©

is a plush, disk-based program that maintains your class rolls in a disk file; allows you to enter grades, add, delete or edit, compute class averages, alphabetize, line-print, assign grades, display a histogram, and much more.

You can enter new grades without having to alphabetize your papers or enter the student's names or look up anything in a directory!

For TRS-80* with one disk and 32K: $39.95.

Order from:

Report Card
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16 K X 1 DYNAMIC RAMS MK4116P3
- 200 NSEC ACCESS/375 NSEC CYCLE TIMES
- 16 PIN/TTL COMPATIBLE
- ALL CHIPS BURNED IN AND FULLY TESTED
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6800/6502 64K BYTE RAM & CONTROLLER SET
MAKE 64K BYTE MEMORY FOR YOUR 6800 OR 6502
THIS SET INCLUDES:
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- DATA & APPLICATION SHEETS. PARTS TESTED AND GUARANTEED.
  S295.00 PER SET

DYNAMIC MEMORY CONTROLLER MC3480L
- GENERATES RAS/CAS & REFRESH TIMING FOR 16K TO 64K BYTE MEMORIES
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- MUX ADDRESS & REFRESH COUNTER FOR 16K TO 64K BYTE MEMORIES
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MEMORY DEVICES DIVISION
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8048 Family

A one board microcomputer utilizing the 8035 geared toward stand alone applications with:
- one 8-bit input port
- one 8-bit output port
- one 8-bit bidirectional port
- fully programmable hand shake lines on each port
- crystal based timer
- 64 bytes RAM, expandable to 1k bytes
- provisions for program memory to 4k bytes
- single supply capability [+5V]
- low cost [64.95 - singles]

Money order, Check, or C.O.D.
Send orders to:

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Columbus, Ohio 43215
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Circle 5 on inquiry card.

...add the sound dimension to your system

NOISEMAKER!

Soundboard uses two GI AY 3-8910 I.C.'s to generate sound effects under software control. PCB only $34.95.

Send for additional information, check or money order to:

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Elmhurst, Illinois 60126
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Circle 7 on inquiry card.

tinyFORTH

tinyFORTH is a powerful interactive programming system for the TRS-80. tinyFORTH combines the structured high-level language, text editor, and assembler of FORTH with the graphics and cassette I/O of the TRS-80.

tinyFORTH programs are quickly developed by defining new modules in terms of previously defined modules. Each new module is compiled for fast execution and compact memory space.

tinyFORTH is easy to learn. The user's manual contains hundreds of examples to teach you tinyFORTH in a hands-on style. Special chapters explain graphics, applications, the text editor, and the assembler.

tinyFORTH cassette for 16k level II TRS-80 and full documentation $29.95
Documentation only $9.95

All orders are fully guaranteed. Add $1.50 for postage and handling. Order with check, money order, Visa, or Mastercharge.

The Software Farm
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Business Software Pkg. ... 625.00	Apple Radio Car 159.00
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★ Front Panel
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MEMORY EXPANSION KITS
4116's
16K (200/250 ns.)
8 pcs. for **$74.95**
w/instructions & jumpers.

EXIDY SORCERER ONLY $799.00



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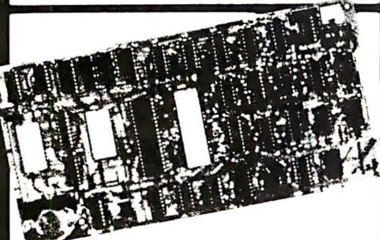
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Z-80 based singleboard computer by SD Systems

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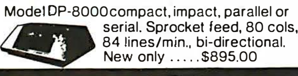
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2111	3.75	3.65	3.55
2112-1	2.95	2.65	2.65
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8080A CPU	34.95
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16K Static RAM (2114)	29.95
32K Static RAM (2114)	49.95
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9 Slot Mother Board (WMC)	29.95
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NOTICE: WE DO CUSTOM PROM PROGRAMMING

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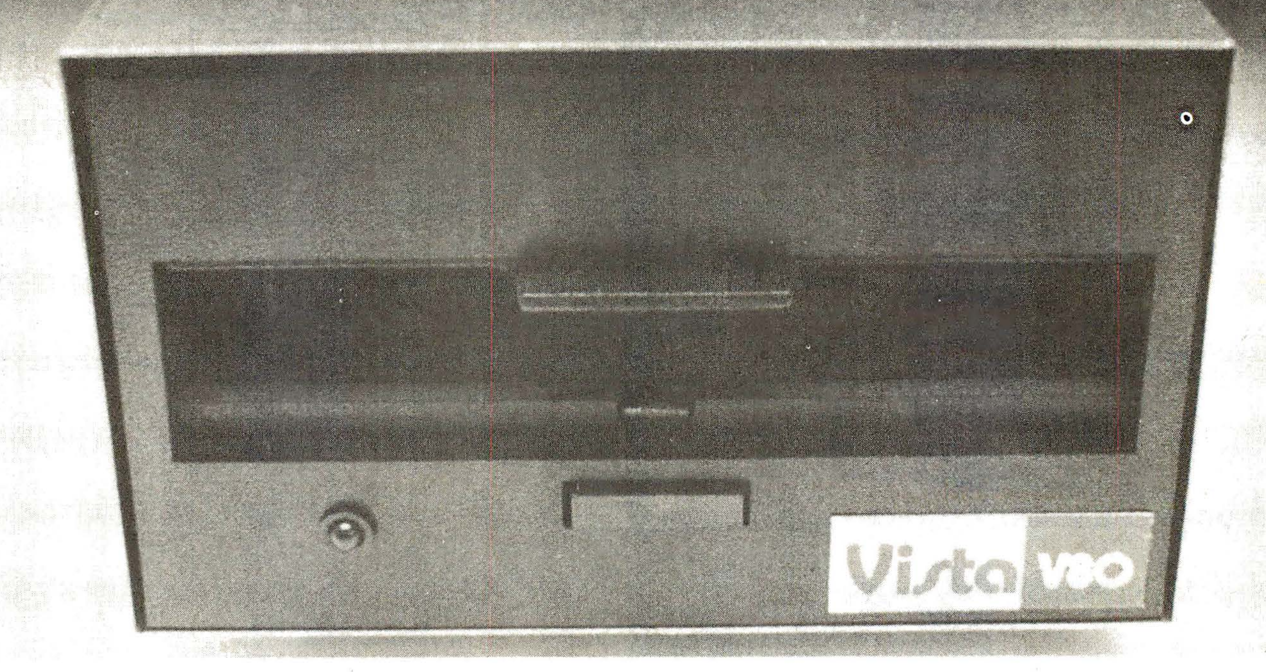
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The Vista V80: $395

The Vista V80 Mini Disk System is the perfect way to widen the capabilities of your TRS-80* Microcomputer. Quickly and inexpensively. Our $395 price tag is about $100 less than the Radio Shack equivalent. Our delivery time is immediate (24 hour turn-around from our Santa Ana, Ca. factory). And our system is fully interchangeable. That's just the start.

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It has a better warranty than any comparable unit warranty available – a full 120 days on all parts and service. When you consider how much more goes into the Vista V80, that shows a lot of faith in our product.

A full 3 amp power supply means you have 2½ times the power necessary to operate the V80, and full ventilation insures that there will be no problems due to overheating.

The Vista V80 Mini Disk System requires Level II Basic with 16K RAM Expansion interface (it operates from the Radio Shack interface system. It comes complete with a dependable MPI Minifloppy disk drive, power supply, regulator board and vented case. It's shipped to you ready to run – simply take it out of the box and plug it in. You're in business. From the company that means business – Vista Computer Company.



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Manufacturers of Quality Computer Systems and Software.

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Circle 381 on inquiry card.

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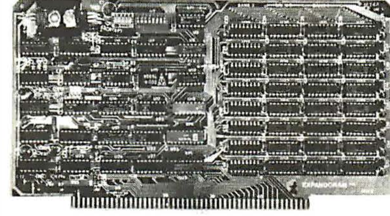


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SD EXPANDORAM



The EXPANDORAM is available in versions from 16K up to 64K, so for a minimum investment you can have a memory system that will grow with your needs. This is a dynamic memory with the invisible on-board refresh, and IT WORKS!

- Bank Selectable
- Phantom
- Power 8VDC, +16VDC, 5 Watts
- Lowest Cost Per Bit
- Uses Major Brand 16K RAMS
- PC Board is doubled solder masked and has silk-screened parts layout
- Extensive documentation clearly written

- Complete kit includes all Sockets for 64K
- Memory access time: 375ns, Cycle time: 500ns.
- No wait states required
- 16K boundaries and Protection, via Dip Switches
- Designed to work with Z-80, 8080, 8085 CPU's

EXPANDORAM 64K Kit (16K Ram)

WITHOUT MEMORY $139.00
16K 209.00
32K 275.00
48K 340.00
64K 405.00

SD'S PROM 100 PROM Programmer Board

The PROM-100 Programmer is a development tool for S-100 Bus computer systems. The Zero Insertion Force Programming Socket extends above the card cage height for easy access to PROM devices. Software verifies PROM erasure, verifies program loading and provides for reading of object file from Disk or PROM and programming into PROM/EPROM. Features include: On-board generated 25vdc Programming pulse, TTL compatible, maximum programming time for 16,389 bits is 100 seconds. Programs: 2708, Intel 2758, 2716, 2732 and TI 2516. DIP Selectable EPROM type.

PROM-100 Board Kit $149.95

SD'S MPB-100 Z80 CPU BOARD KIT



The MPB-100 provides, a Z80 microprocessor based CPU for S-100 Bus systems. Front panel usage is optional, making the MPB-100 suitable for upgrading existing systems to Z80 level. A PROM socket is provided on-board which makes the MPB-100 adaptable to process control applications. Features include: Power-on Jump to 4K boundaries, 2 Megahertz or 4 Megahertz operation, optional wait states, on-board PROM socket.

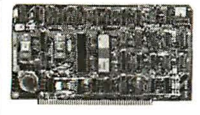
MPB-100 KIT $199.00

SD'S VERSAFLOPPY II

• IBM 3740 Compatible Soft Sectored Format for Single Density Drives • Operates with Single and Dual Sided Drives. Single or Double Density Drives and 5" & 8" Drives — in any combination of four simultaneously • Drive Select and Side Select Circuitry • S-100 Bus Compatible • Vectored Interrupt Operation Optional • Phase Locked Loop Data Recovery Circuit • Operates with Z80 CPU's • Uses FD1791-1 Controller Chip • Ther Versafloppy II incorporates all the possible features of a flexible disk drive controller into one board. Capable of handling four drives simultaneously, combinations of any variety are possible, such as 5" single sided, 8" dual density dual sided, 5" dual density single sided. Most popular drives are controlled directly with the Versafloppy II. The operating system for the Versafloppy II is the extremely powerful SDOS available for SD Systems. Diagnostic and control software available to complete your disk system.

$290 KIT, $385.00 ASSEMBLED & TESTED

SD'S VDB-8024 VIDEO DISPLAY BOARD



The VDB-8024 features its own on-board Z80 microprocessor. This gives the capability of using software (included in ROM) to control functions and enhancements without interference with the computer's CPU. Included in the special features: 80 characters by 24 lines display, keyboard power and interface, composite and separate video output, 2K on-board RAM, a total of 256 available characters, full cursor control, forward and reverse scrolling, underlining, field reverse, field protect enhancements, programmable characters. **VDB-8024 KIT $289.00**

SD'S "VERSAFLOPPY I" KIT

FEATURES: IBM 3740 soft sectored compatible, S-100 BNS Compatible for Z-80 or 8080. Controls up to 4 drives (single or double sided). Directly controls the following drives: Sugart SA400/450 Mini Floppy • Shugart SA800/850 Standard Floppy • PERSCI 70 and 277 • MFE 700/750 • CDC 9404/9406

$135.00

SD'S SBC-100 SINGLE BOARD COMPUTER

The SBC-100 provides a complete micro-computer on a single board! The Z80 microprocessor is used as the heart of the SBC-100. The SBC-100 meets all the requirements of a Z80 CPU board with the added features of I/O ports, counter/timer channels, on board RAM, provisions for PROM/ROM and a software programmable baud rate generator. S-100 Bus compatible, the SBC-100 features are: 8K bytes of available PROM, 1024 bytes on-board RAM, Serial I/O with both synchronous and asynchronous operation. Parallel I/O ports, Operational Vectored Interrupts, and Four Counter/Timer Channels. SD Monitor available for RS-232 and Video Terminals. Disk based system software also available.

SBC-100 KIT $209.00

TARBELL FLOPPY DISK INTERFACE

Compatible with Z80 & 8080. S-100 Bus. Uses CPM operating system. Plugs directly into your IMSAI or ALTAIR • Fastest transfer rate
KIT $190.00 Assembled & Tested $260.00

TARBELL CASSETTE INTERFACE

Plugs directly into your IMSAI or ALTAIR • Fastest transfer rate • Extremely reliable • Phase encoded • 4 extra status & control lines
KIT $99.95

COMPUTER CORNER

CPU'S

Z80	$10.99
RELATED CHIPS	
2114 (300ns)	$5.99
Z80 PIO	$9.95
2708	$7.99
4115	8/$34.95
4116	8/$80.00
DISC CONTROLLER	
1771	$29.95
1791	$37.95

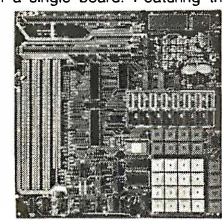
IC SOCKETS

SOLDER TIN PIN		LOW PROFILE PIN	
8	.12	16	.17
14	.15	18	.24
24	.32	40	.54
28	.39	20	.26

Z80 STARTER KIT

Kit: $219.95 Assembled & Tested $369.95

SD System's Z80 Starter Kit enables the novice to build a complete microcomputer on a single board. Featuring the powerful Z80 microprocessor, the Z80 Starter Kit features • Keyboard and Display • Audio Interface • PROM Programmer • Expansion and Wire Wrap Area • On Board RAM • 4 Channel Counter/Timer • Z-BUG Monitor in PROM • I/O Ports.



DIP SWITCHES

3 Pos.	$1.10
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8 Pos.	$1.26
9 Pos.	$1.36
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4N27	1.10
4N28	.95
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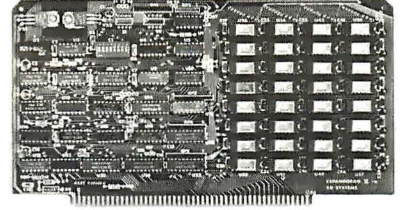
S-100 CONNECTORS

High-Quality Gold Pins
$2.99 EACH

FLOPPY DISK SPECIAL

5.25" SOFT, 10 OR 16 SECTOR
10 FOR $29.95
8" SOFT SECTORED IBM COMPATIBLE
10 FOR $34.95

SD'S EXPANDORAM II
The Randem Access Memory



- S-100 Bus Compatible
- Up to 4Mhz Operation
- Expandable Memory from 16K to 256K
- DIP Switch Selectable Boundaries
- Uses 16K (4116) or 64K (4164) Memory Devices
- Page Mode Operation Allows up to 8 Memory Boards on Bus
- Operates with Z80 CPU's
- Phantom Output Disable
- Invisible Refresh (Synchronized with Wait States)

SD Systems' ExpandoRAM II is a dynamic RAM board with capacities from 16K bytes (4116) to 256K bytes (4164). It operates on the industry S-100 Bus. The design allows 8 boards to operate from the same S-100 Bus. The ExpandoRAM II is compatible with most S-100 CPU's based on the Z80 microprocessor.

EXPANDORAM II KIT

W/O $195.00
16K 285.00
32K 375.00
48K 465.00
64K 555.00

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ABBREVIATIONS: S/T Solder Tail; S/E Sold. Eyelet: W/W Wire Wrap 3; SW/W Short W/Wrap;

PART #	Description	Row Sp.	1-4	5-9	10-24
5010	50/100 S/T ALTAIR	.140	3.75	3.50	3.30
5020	50/100 S/T IMSAI	.250	3.95	3.75	3.50
5030	50/100 W/W IMSAI	.250	4.10	3.90	3.70
5040	50/100 S/E ALT/IMSAI	.140	5.00	4.50	4.25
5050	50/100 S/T CROMEMCO	.250	6.25	6.00	5.75
1450	IMSAI CARD GUIDES		0.16	0.14	0.12
.100" Contact Center Connectors.					
1020	13/26 S/E Imsai MIO:	.140	2.10	1.85	1.75
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1050	25/50 S/T	.140	3.00	2.80	2.60
1060	36/72 W/W Vector.	.200	4.80	4.60	4.30
1065	36/72 S/T Vector.	.200	4.00	3.75	3.50
1070	40/80 S/E PET	.140	4.80	4.50	4.30
1075	40/80 W/W PET	.200	5.00	4.65	4.35
1080	40/80 S/T PET	.140	4.90	4.60	4.25
1085	43/85 S/E Cos.ELF	.140	5.00	4.75	4.50
1090	43/86 S/T Cos.ELF	.140	5.10	4.85	4.60
1093	43/86 S/T Cos.ELF	.200	4.95	4.70	4.45
1095	43/86 W/W Cos.ELF	.200	5.50	5.20	4.90
POLARIZING KEYS: For Above			0.10	0.10	0.10
.156" Contact Center Connectors.					
1550	6/- S/E PET,Etc	.140	1.30	1.10	0.90
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1580	12/24 S/T PET	.140	2.10	1.90	1.70
1590	15/30 S/E GRI Keybd.	.140	2.25	2.05	1.85
1620	18/36 S/E	.140	2.40	2.20	2.00
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1710	36/72 S/E	.140	3.50	3.30	3.10
1720	36/72 S/T	.200	3.30	3.10	2.90
1730	43/86 S/T Mot. 6800	.140	4.40	4.15	3.90
1740	43/86 S/T Mot. 6800	.200	4.35	4.10	3.85
1750	43/86 W/W Mot. 6800	.200	4.45	4.25	4.10
POLARIZING KEYS: For Above			0.10	0.10	0.10

RS232 & 'D' TYPE SUBMINIATURE CONNECTORS:

QUANTITY		1-4	5-9	10-24
DE9P Male		1.45	1.35	1.25
DE9S Female		1.93	1.80	1.70
DE110963-1	2pc. Grey Hood	1.20	1.10	1.00
DA15P Male		1.95	1.80	1.70
DA15S Female		2.80	2.60	2.40
DA51211-1	1pc. Grey Hood	1.25	1.15	1.10
DA110963-2	2pc. Grey Hood	1.22	1.10	1.05
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DB25S Female		3.20	3.00	2.70
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DB51226-1A	2pc. Black Hood	1.40	1.30	1.20
DB110963-3	2pc. Grey Hood	1.35	1.25	1.15
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DC37S Female		4.90	4.70	4.40
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DD50S Female		4.90	4.70	4.50
DD51216-1	1pc. Grey Hood	2.30	2.10	1.90
DD110963-5	2pc. Grey Hood.	2.40	2.20	2.00
D20418-2 Hardware Sets		0.75	0.70	0.65

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2708 EPROMS PRIME
$14.00 ea.

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Price: $9.00ea. 5 pcs. $7.50ea.

WHISPER FANS: Excellent for Computer cabinet cooling. Extremely quiet.
Dim. 4-3/4" x 1-1/2" thick. U.L. Listed.

1-4	5-9	10-24
$22.00	$19.00	$18.00

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4002	.22	4025	.22	4071	.20	74C151	1.75
4007	.27	4027	.45	4072	.35	74C157	1.75
4009	.45	4028	.80	4081	.22	74C160	1.20
4010	.45	4029	.95	4520	1.00	74C163	1.00
4011	.22	4030	.35	74C00	.27	74C165	1.25
4012	.22	4035	.97	74C02	.27	74C173	1.30
4013	.40	4042	.85	74C08	.30	74C174	1.20
4014	1.20	4044	.85	74C10	.27	74C175	1.20
4015	1.00	4045	.45	74C14	1.20	74C192	1.30
4016	.45	4046	1.95	74C20	.27	74C193	1.40
4017	1.05	4049	.75	74C42	.90	74C901	.50
4018	.90	4050	.45	74C73	.75	74C902	.50
4019	.45	4051	1.10	74C74	.50	74C914	1.90
4020	1.10	4053	1.10	74C83	1.30		
4021	1.10	4055	1.25	74C86	.50		
4022	1.00	4066	.70	74C90	.95		
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2716(T13 VOLTAGES	35.95	82S131	3.95
2716 (Intel) +5V	55.95	AY5 1013 VART	5.25
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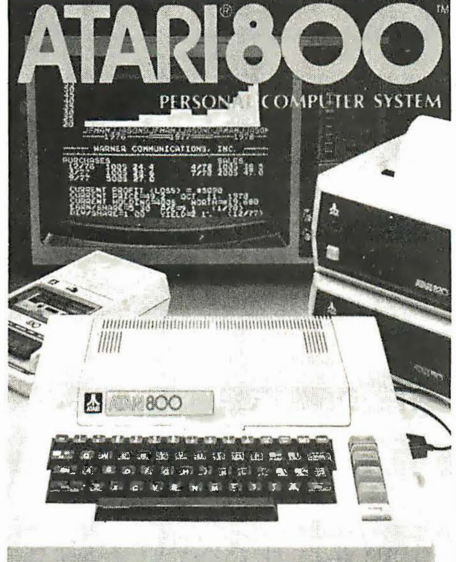
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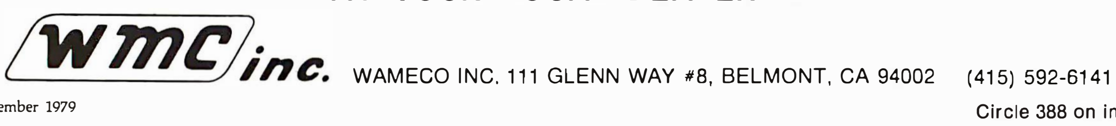
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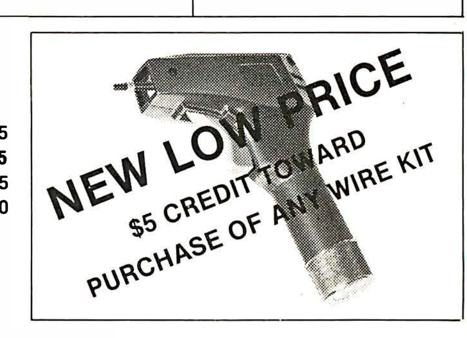
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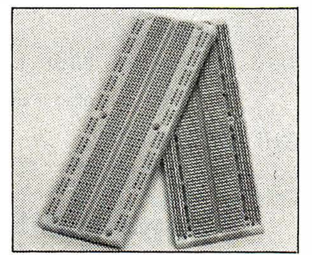
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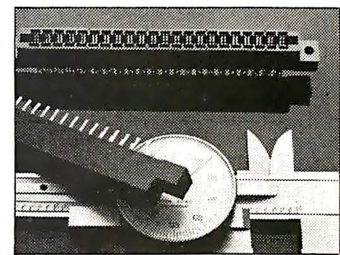
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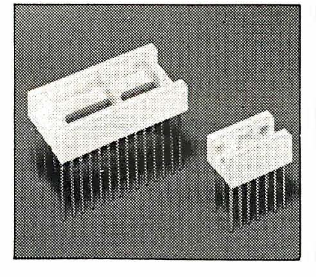
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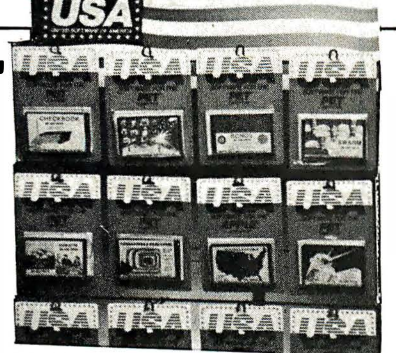
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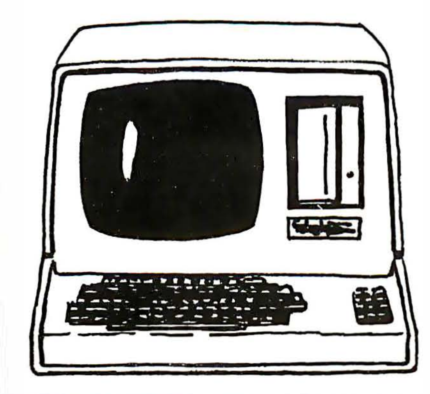
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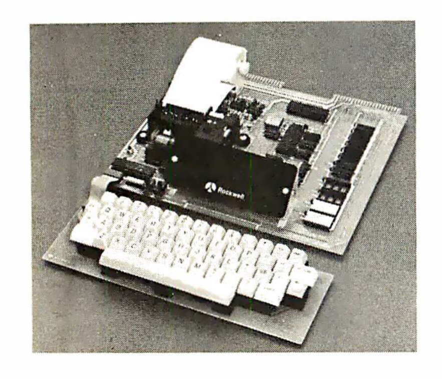
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AIM 65

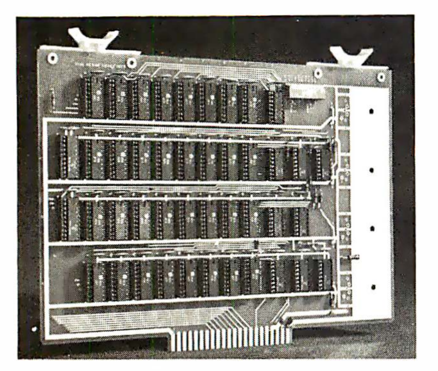
AIM 65 is fully assembled, tested and warranted. With the addition of a low cost, readily available power supply, it's ready to start working for you. It has an addressing capability up to 65K bytes, and comes with a user-dedicated 1K or 4K RAM.

- **Thermal Printer**
- **Full-Size Alphanumeric Keyboard**
- **True Alphanumeric Display**
- **Proven R6500 Microcomputer System Devices**
- **Built-In Expansion Capability**
- **TTY and Audio Cassette Interfaces**
- **ROM Resident Advanced Interactive Monitor**
- **Advanced Interactive Monitor Commands**

PRICE: $375.00(1K RAM)

Plus $4.00 UPS (shipped in U.S. must give ***street*** address), $10 parcel post to APO's, FPO's, Alaska, Hawaii,Canada, $25 air mail to all other countries

We manufacture a complete line of high quality expansion boards. Use reader service card to be added to our mailing list, or U.S. residents send $1.00 (International send $3.00 U.S.) for airmail delivery of our complete catalog.



VAK-4 DUAL 8K-RAM $379.00
VAK-2 8K-RAM (½ populated) **$239.00**

VAK-4 16K STATIC RAM BOARD

- Designed specifically for use with the **AIM-65**, **SYM-1**, and **KIM-1** microcomputers
- Two separately addressable 8K-blocks with write protect
- Designed for use with the **VAK-1** or **KIM-4*** motherboards
- Has provisions for mounting regulators for use with an unregulated power supply
- Made with 1st quality 2114 static ram chips
- All IC's are socketed
- Completely assembled, burned-in, and tested

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② Line Printer
③ Mini Disk System
④ C-10 Cassettes
⑤ Verbatim Diskettes





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ITEM		REG. PRICE	OUR PRICE
Level II—4k		$619.00	$575.70
Level II—16k		$849.00	$789.60
Expansion Interface		$299.00	$278.00
Mini Disk Drive		$ 495.00	$ 385.00
Centronics 779 Printer		$1599.00	$1175.00
Centronics 101 Printer		$1595.00	$1400.00
Anadex DP-8000 Printer		$1295.00	$ 995.00
Memory Kit (16K) FREE INSTALLATION		$ 149.00	$ 98.00
Verbatim Diskettes ea.		$ 5.95	$ 4.95
	3	$ 17.89	$ 12.00
	10	$ 59.00	$ 37.00
C-10 Cassettes	5	$ 4.95	$ 4.50
	25	$ 24.75	$ 18.75
Paper (9½" x 11" fanfold, 3500 sheets)		$ 35.00	$ 29.95

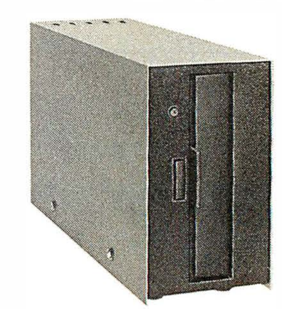
Centronics 730 $850.00
Same as Line Printer II

TRS—80 MODEL II $ 3208.50
- **32K RAM**
- **½ MEG DISK**

ADDITIONAL 32K RAM	$ 418.50
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ADDITIONAL DISK DRIVE (2ND + 3RD)	$ 558.00

MINI DISK DRIVES NOW $385

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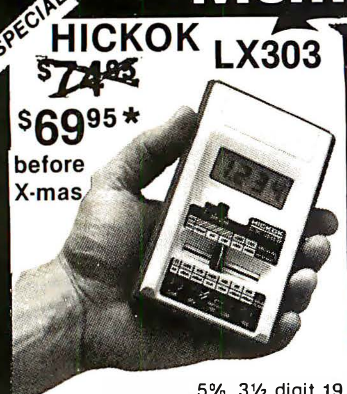
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.5%, 3½ digit 19 Range DVM. ½" LCD displays runs 200 hrs on 1 battery. 10 Meg Ohm Input. 1 yr. guarantee, made in U.S.A., test leads included.

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- **VP-40** 40Kv DC Probe **$35.00**
- **CS-1** 10 Amp Current Shunt **$14.95**

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Just for Asking.

FREE BATTERY with your meter.

RS232 & "D" TYPE CONNECTORS *

P = Plug-Male S = Socket-Female C = Cover-Hood

PART NO.	DESCRIPTION	PRICE 1-4	5-9	10-24
DE-9P	9 Pin Male	1.50	1.30	1.20
DE-9S	9 Pin Female	2.15	2.05	1.95
DE-9C	9 Pin Cover	1.50	1.30	1.15
DA15P	15 Pin Male	2.20	2.00	1.80
DA15S	15 Pin Female	3.20	3.00	2.80
DA15C	15 Pin Cover	1.60	1.45	1.30
DB-25P	25 Pin Male	2.90	2.60	2.50
DB-25S	25 Pin Female	3.75	3.65	3.40
DB51212-1	1 pc. Grey Hood	1.65	1.40	1.20
DB1226-1A	2 pc. Black Hood	1.90	1.60	1.50
DB110963-3	2 pc. Grey Hood	1.80	1.55	1.35
DC37P	37 Pin Male	3.95	3.80	3.60
DC37S	37 Pin Female	5.75	5.50	5.20
DC37C	37 Pin Cover	2.20	1.95	1.75
DD50P	50 Pin Male	4.95	4.75	4.50
DD50S	50 Pin Female	7.50	7.20	6.90
DD50C	50 Pin Cover	2.50	2.20	2.10
D20418-S	Hardware Set (2 pair)	1.00	.80	.70

MALE

FEMALE

Connector for CENTRONICS 700 SERIES:
Amphenol 57-30360 for back of Centronics 700 Series printers
1-4—$9.00 5-up—$7.50

SALE S-100 BUS EDGE CONNECTORS * SALE

S100-WWG 50/100 Cont .125 ctrs. 3 LEVEL WIRE WRAP .025" sq. posts on .250 spaced rows. GOLD PLATED

1-4	5-9	10-24
$4.75	$4.00	$3.75

S100-STG 50/100 Cont .125 ctrs. DIP SOLDER TAIL on .250 spaced rows for VECTOR, IMSAI, CROMENCO mother boards GOLD plated

1-4	5-9	10-24
$4.10	$3.80	$3.50

S100SE 50/100 Cont .125 ctrs. PIERCED SOLDER EYELET Tails GOLD

1-4	5-9	10-24
$5.00	$4.50	$4.00

S100ALT 50/100 Cont .125 ctrs. DIP SOLDER TAIL on .140 spaced rows for ALTAIR motherboards, GOLD plated.

1-4	5-9	10-24
$4.50	$4.25	$4.00

Other Popular Edge Connectors

D2244-5WW 22/44 Cont .156 ctrs. WIRE WRAP tails GOLD.

1-4	5-9	10-24
$3.95	$3.70	$3.40

D2244-5SE 22/44 Cont .156 Ctrs. PIERCED SOLDER EYELET tails GOLD plated.

1-4	5-9	10-24
$3.00	$2.60	$2.20

CG 1 (MSA) Style Card Guides 5/$1.00

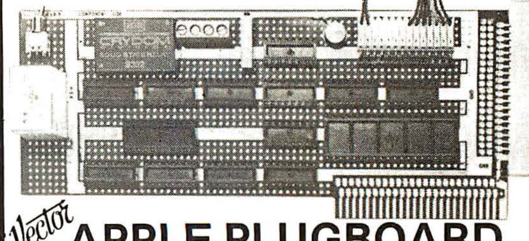
See our July Ad for many other connectors.

3 LEVEL GOLD WIRE WRAP SOCKETS*

Sockets purchased in multiples of 50 per type may be combined for best price.

	1-9	10-24	25-99	100-249	250-999
8 pin	.40	.36	.34	.31	.27
14 pin	.44	.43	.41	.39	.37
16 pin	.55	.47	.45	.41	.39
18 pin	.70	.60	.55	.50	.45
20 pin	.90	.80	.75	.65	.62
22 pin	.95	.85	.80	.70	.65
24 pin	.95	.85	.80	.70	.65
28 pin	1.25	1.15	1.00	.95	.90
40 pin	1.65	1.45	1.35	1.20	1.10

All sockets are GOLD 3 level closed entry. 2 level Tail Low Profile, Tin Sockets and Dip Plugs available. CALL FOR QUOTATION.



Vector APPLE PLUGBOARD

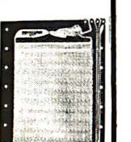
Vector 4609 Peripheral Interface Plugboard for construction of custom circuits. Plug compatible with Apple II, Commodore PET and Super Kim microcomputers. Three connectors, in addition to the standard 25/50 system bus, are available for input/output. A 20/40-contact card-edge connector, fabricated on the rear of the board, mates with a 3-M type ribbon connector. Alternatively, a right-angle solder-tail header may be positioned in this same location. The Model 4609 also accomodates the miniature SIP-type connectors which may be placed on the periphery or in mid-board.

1-4	5-9	10-24
$21.50	$19.36	$17.26

7520 APPLE EXTENDER CARD $24.95

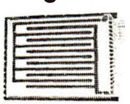
8803 MOTHER BOARD FOR S100 BUS MICRO-COMPUTERS — Vector

- Kit includes 12 tantalum capacitors for +5, +12, —12 buses and insulated mounting spacers
- Wiring side shown. Component side bare epoxy glass with white markings for component locations
- G10 epoxy glass board with 2 ounce copper, solder plated and .038 diameter holes for leads.
- Solder mask with solder windows on etched circuits to avoid accidental short circuits
- Mounts 11 receptacles with 100 contacts (2 rows) on .125 centers with .250 row spacing. Vector part number R681-2, or mounts 10 receptacles plus interconnections to smaller mother board for expansion
- Includes etched circuits and instructions for option of active, pull-up, or floating terminations
- Large buses +5V and GND (10 AMPS), ±12V or 16V (2 AMPS). Current ratings are per MIL-STD-275 with 10°C rise
- Fits in Vector-pak enclosures
- Fits in IMSAI 8080 microcomputer as expander board



Price: $29.50

Vector Plugboards



8800V

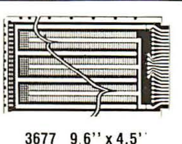
Universal Microcomputer/processor plugboard, use with S-100 bus. Complete with heat sink & hardware. 5.3" x 10" x 1/16"

1-4	5-9	10-24
$19.95	$17.95	$15.96

8801-1

Same as 8800V except plain; less power buses & heat sink.

1-4	5-9	10-24
$15.22	$13.79	$12.18



3682 9.6" x 4.5" **$12.97**

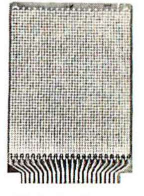
3682-2 6.5" x 4.5" **$9.81**

Hi-Density Dual-In-Line Plugboard for Wire Wrap with Power & Grd. Bus Epoxy Glass 1/16" 44 pin con. spaced .156

3677 9.6" x 4.5" **$10.90**

3677-2 6.5" x 4.5" **$9.74**

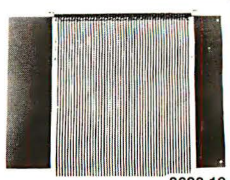
Gen. Purpose D.I.P. Boards with Bus Pattern for Solder or Wire Wrap. Epoxy Glass 1/16" 44 pin c n. spaced .156



3662 6.5" x 4.5" **$8.95**

3662-2 9.6" x 4.5" **$11.45**

P pattern plugboards for IC's Epoxy Glass 1/16" 44 pin con. spaced .156



3690-12

CARD EXTENDER

Card Extender has 100 contacts 50 per side on .125 centers-Attached connector-is compatible with S-100 Bus Systems. **$25.83**

3690 6.5" 22/44 pin .156 ctrs. Extenders $13.17

1/16 Vector BOARD



.042 dia holes on 0.1 spacing for IC's

		PRICE	
Phenolic			
PART NO.	SIZE	1-9	10-19
64P44XXXP	4.5x6.5"	$1.56	$1.40
169P44XXXP	4.5x17"	$3.69	$3.32
Epoxy Glass			
64P44	4.5x6.5"	$1.79	$1.61
84P44	4.5x8.5"	$2.21	$1.99
169P44	4.5x17"	$4.52	$4.07
169P84	8.5x17"	$8.83	$7.95

TRS-80/APPLE MEMORY EXPANSION KITS

4116's RAMS from Leading Manufacturers

1,000's SETS SOLD! 100% GUARANTEED

(16Kx1 200/250ns)

8 for $75.00

Add $3.00 for programming Jumpers for TRS-80 Keyboard

3M SCOTCH® BRAND DISKETTES

Part No.	Sides/ Density	Sectoring	Price Box of 10
		8"	
740-OP	1/single	Soft-IBM	$39.95
740/2-OP	2/single	Soft-IBM	$75.00
740-32P	1/single	32	$39.95
740/2-32P	2/single	32	$75.00
741-0	1/double	Soft	$59.00
		5"	
744-OK	1/single	Soft-(TRS-80)	$51.00*
744-10K	1/single	Soft/10	$51.00*
744-16K	1/single	Soft/16	$51.00*

*Price includes Kas-ette/10 Storage Box a $5.00 Value (TRS-80)

"DON'T SETTLE FOR ANYTHING LESS THAN SCOTCH"

WOW



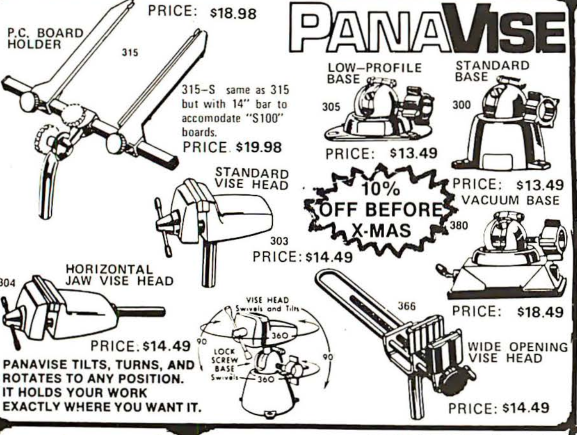
14 & 16 PIN GOLD 3 LEVEL WIRE WRAP SOCKES*

14 - G3 100 for **$36.00**

16 - G3 100 for **$37.00**

50 of each for **$38.00**

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PANAVISE TILTS, TURNS, AND ROTATES TO ANY POSITION. IT HOLDS YOUR WORK EXACTLY WHERE YOU WANT IT.



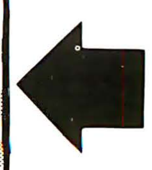


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MEMORY MEMORY

2102LIPC	Low Power 450ns in lots of 25	$1.10
2102AL-2	Low Power 250ns in lots of 25	$1.25
2114-3L	1Kx4 300 ns Low Power	8/$50.00
5257-3L	4Kx1 300ns Low Power	8/$50.00
2708	8K 450ns EPROM	8/65.00 $9.00
2716	16K 5 Volt Only EPROM	$40.00

CALL FOR QUANTITY PRICES







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IM-10A List $89.00
SPECIAL
$56.95 with tube

Perfectly balanced fluorescent lighting with precision magnifier lens. Tough thermoplastic shade. Easy lens removal. New wire clip design permits easy installation and removal of fluorescent tube. Comes with plastic shield to protect tube from soiling and damage.

Colors: Gray, Black, and Chocolate Brown. Comes with one 22 watt T-9 Circline fluorescent tube. 3 diopter lens.

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Vector WRAP POST

for .042 dia. holes (all boards on this page)

- **T44/C** pkg. 100 .. **$ 2.34**
- **T44/M** pkg. 1000 ..... **$14.35**
- **A-13** hand installing tool .... **$ 4.19**

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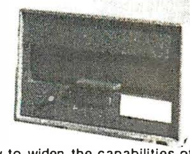
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MEMORY WAR SHOP AND COMPARE

LOOK FOR OUR HUGE AD IN JANUARY BYTE

The Vista V80: widen the ability of your TRS-80 $395.00



The Vista V80 Mini Disk System is the perfect way to widen the capabilities of your TRS-80* Micro-computer. Quickly and inexpensively. Our $395 price tag is about $100 less than the Radio Shack equivalent. Our delivery time is immediate. And our system is fully interchangeable. That's just the start.

It will give you 23% more storage capacity by increasing useable storage from 55,000 to 65,000 bytes per drive with our new software patch.

It can work 8 times faster than the TRS-80 Mini-Disk system, because track-to-track access is 5ms versus 40ms for the TRS-80. You can realize this added speed once the new double disk expansion interface is available without expensive modification of the existing unit.

It has a better warranty than any comparable unit warranty available - a full 120 days on all parts and service. When you consider how much more goes into the Vista V80, that shows a lot of faith in our product.

A full 3 amp power supply means you have 2½ times the power necessary to operate the V80, and full ventilation insures that there will be no problems due to overheating.

The Vista V80 Mini Disk System requires Level II Basic with 16 K RAM Expansion interface (it operates from the Radio Shack interface system. It comes complete with a dependable MPI Minifloppy disk drive, power supply, regulator board and vented case. It's shipped to you ready to run-simply take it out of the box and plug it in. You're in business. From the company that means business - Vista Computer Company.

DATA CABLES, VC80-2 (2 drive) $29.95
DATA CABLES, VC80-4 (4 drive) $39.95

SPECIAL: Box of 10 diskettes - $20.00 with Purchase of VISTA 80

SAVE $100.00 DM2700S DISK & CABINET with POWER SUPPLY



DM2700S includes Siemens FD120-8" Disk Drive with the following features:

- Single or Double Density
- Hard or Soft Sector
- Door Interlock
- Write Protect
- Hard Sector Detection
- 500 KB/S Transfer
- 800 KB unformated
- Bit density 6536 BPI
- Shugart 800 Series Compatable

Cabinet includes:

- 110V to 125V 60 Hz power supply
- Data Cable
- Fan
- Accepts per SCI, Shugart, Siemans 8" Drives

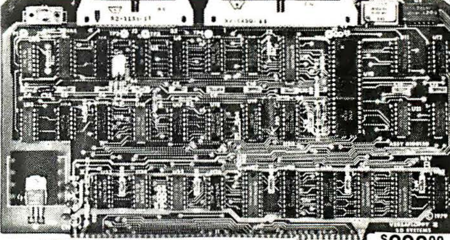
SHOP AND COMPARE
DM2700S Disk Drive & Cabinet
Reg.$750 Sale Priced **$650**

FDD120-8 $449.00
DM2700 Cabinet, less Drive
Reg.$249 Sale Priced **$225.00**

NEW VERSAFLOPPY II NEW
DOUBLE DENSITY, DOUBLE SIDED, DISC.CONTROLLER

GENERAL DESCRIPTION:
Versafloppy II is a flexible disk drive controller that incorporates a wide range of capabilities into one board. It operates with double density soft sectored format which provides 985,600 bytes of storage on a double sided 8 inch diskette and 129,920 bytes per side on a five inch mini-diskette. The Versafloppy II directly controls many popular disk drives. These include: Shugart SA400 and SA450; Shugart SA800 and SA850; Mayflower MFE500 and MFE700; Per Sci 70 and 277; and Siemans, BSI-105.

- S-100 Bus IEEE Standard Compatible
- IBM-3740 Compatible Soft Sectored Format for Single Density Drives
- Operates with both Standard (8") and Mini (5") Drives Simultaneously
- Provides Control for Double Sided Operation
- Operates with Z80, 8080, and 8085 Central Processing Unit
- Controls up to four drives
- Vectored Interrupt Operation Optional
- Control and Diagnostic Software Available in PROM
- SDOS Disk Operating System Compatible



SDS-VERSAFLOPPY II KIT ~~$309.00~~ $290.00
SDS-VERSAFLOPPY II A&T ~~$399.00~~ $390.00

M-XVI
The true 16K Static Ram module for S-100 bus systems.
ASSEMBLED & TESTED -- 100% BURN IN

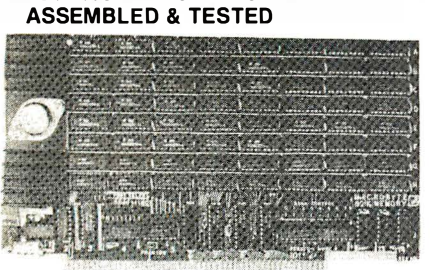
SHOP & COMPARE SPECIAL

California Computer Systems

The M-XVI gives you unbelievable expansion capabilily for your S-100 bus system-even beyond 64K. Manufactured to the highest industry standards documented and designed to make assembly, use, and programming a snap. The M-XVI board is a true revelation for the serious hobbyist and use in practical business or industrial applications.

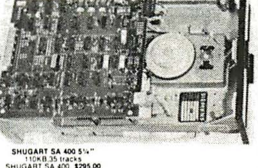
FEATURES:

- Fully static
- Uses popular 2114 static RAMS
- +5 volt operation only
- Bank Select available by bank port and bank byte
- Phantom line capability
- Addressable in 4K blocks
- 4K blocks can be addressed any where within 64K in 4k increments
- Meets IEEE proposed S-100 signal standards
- LED indicators for board selection and bank selection
- FR-4 epoxy PC boards
- Solder masked on both sides
- Silk screen of part number and part designator



			Sale Priced
2016BA	450ns 2MHZ	Reg.$349.95	$295.00
2016BB	300ns 4MHZ	Reg.$389.95	$329.00
2016BY	Bare Board only		$29.95

DISC DRIVES



SHUGART SA 400 5¼"
110KB,35 tracks
SHUGART SA 400 **$295.00**
SHUGART SA 400
with attractive metal case with cutouts for Data Cable switch, fuse and power cord.
LOBO SA400-C **$325.00**
SHUGART SA400
with Cabinet and Power Supply Assembled, tested & Guaranteed
LOBO SA400-PSC **$395.00**
SHUGART 801R 8"
6.4 megabits, single or double density, hard or soft sector, write protect, and more
SHUGART 801R **$495.00**
Siemens FDD 200-8 8" double sided double density
$850.00

DISC CONTROLLER SD "VERSAFLOPPY" KIT



FEATURES: IBM 3740 Soft Sectored Compatible. S-100 BUS Compatible for Z-80 or 8080. Controls up to 4 Drives (single or double sided). Directly controls the following drives:

1. Shugart SA400/450 Mini Floppy
2. Shugart SA800/850 Standard Floppy
3. PERSCI 70 and 277
4. MFE 700/750
5. CDC 9404/9406
6. GSI/Siemans FDD120-8

34 Pin Connector for Mini Floppy. 50 Pin Connector for Standard Floppy. Operates with modified CP/M operating system and C Basic Computer. The new "Versafloppy" from S.D. Computer Products provides complete control for many of the available Floppy Disk Drives. Both Mini and Full Size. FD1771B-1 Single Density Controller Chip. Listings for Control Software are included in price.
CPM for SD Versafloppy $100.00

The Versatile Floppy Disk Controller
Reg. ~~$159.00~~
ONLY $145.00

THE MICROBYTE M32KSS 32K STATIC MEMORY BOARD ASSEMBLED & TESTED

SAVE $120.00

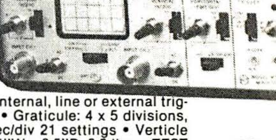
SALE PRICED

M32 KSS-L (2 MHz)
List $650
SALE $530.00

M32 KSS-H (4 MHz)
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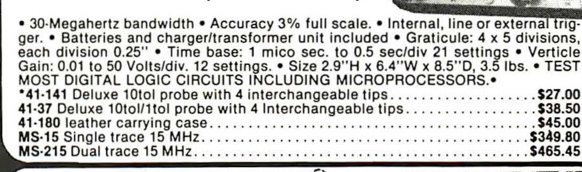
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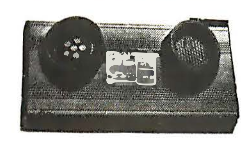
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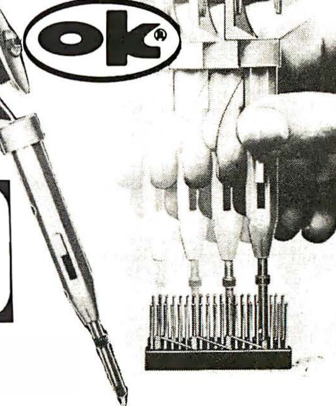
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FOR SALE: Programmatic Flexowriter, paper-tape reader punch, upper/lower case, input/output (I/O) connectors. Some schematics. $370. Bill Fujitsubo, 1506 Sandcastle Dr, Corona del Mar CA 92625.

WANTED: Assembled and working SwTPC PR-40 printer to use with my PET computer. Peter Oakes, 2235 Lakeshore Dr, Muskegon MI 49441.

FOR SALE: Shugart SA3900 dual diskette subsystem. Includes two SA900 drives, SA910 controller electronics, and large enclosure with fan and power supply. 256 K bytes/8 inch drive. Full documentation. Can be used as is, or replace the transistor-transistor logic (TTL) controller with an 8271 chip and your own microcomputer. Cabinet will hold six 8 by 10 inch boards. Original cost $2400, will sell for $750. Roger Cox, 1050 Westmoreland Rd Apt B, Colorado Springs CO 80907, (303) 599-9274.

FOR SALE: New Processor Technology 16 K programmable-memory board with battery backup capability. Never been used. Factory assembled and tested. $250 or best offer. Cromemco Tu-Art, assembled and tested. $200 or best offer. Cromemco Bytesaver, assembled with or without read-only memories (2708), not tested. $175 without read-only memories, $275 with read-only memories including Bytemover Z80 monitor read-only memory. David Brown, 2219 Teresa Dr, Savannah GA 31406.

FOR SALE: Solid State Music MB3 4 K erasable read-only memory board with sixteen clean 1702A read-only memories. Perfect condition, with documentation. $110. George Saum, 4371 W 82 Av, Westminster CO 80030, (303) 429-6646.

FOR SALE: A 2201 Flexowriter made by Friden. The automatic typewriter can be programmed. It has a 5610 Computy data processor mounted in table unit. Has tape punch and reader. Has 18 inch carriage. In good condition. It is a real buy for $800 FOB Newton. Weight 350 to 400 lbs. Jack Harrison, 810 Ridge, Newton NC 28658, (704) 464-0145.

FOR SALE: Alpha-Micro computer system, AM-100, 64 K programmable memory, 10MB CDC Hawk disk drive, AMOS operating system, Accounts Receivable, General Ledger, Payroll Software. Chester Hayes, 62 S Franklin St, Wilkes-Barre PA 18773, (717) 823-3101.

FOR SALE: Litton ABS/1252 accounting computer. System includes 80 K programmable memory, paper-tape reader and punch, keyboard, printer, buffer, rewind stand, and forms stand. Ideal for needs of a small to moderate-size business. David M Martin, 501 Webster, Mishawaka IN 46544, (219) 259-8578 (office) or (219) 259-1123 (home).

FOR SALE: BYTE magazine #1 to current, inclusive. Mint condition. Best offer. K J Dabb, 2045 Robins Av, Ogden UT 84401.

FOR SALE: SOL with 5-slot S-100 cage, 16 K Dynabyte dynamic, 4 K MITS dynamic, 8 K Bytesaver, iCOM minifloppy with controller, cassette recorder, monitor Datel 30 Selectric-based terminal, USART for parallel port, PT Extended Cassette BASIC, iCOM FDOS and DEBBIE, ALS8, Editor, Disassembler, TRK80, and more. Asking minimum $2500. Albert Boulanger, 820 NE 2 Pl, Hialeah FL 33010, (305) 888-6220.

FOR SALE: Parallel ASCII to serial ASCII converter with 20 mA current loop drive, $20; 5 V at 3 A power supply with 45 K μF filtering, $30; miscellaneous power supply components (capacitors, transformers, etc) Robert Watson, 2853 Pebble Beach, Flagstaff AZ 86001, (602) 526-2312.

FOR SALE: Micromation Megabox System, dual drive, 8 inch, double density, with controller card, $1600. Thinker Toys, 16 K static programmable memory, 4 MHz, $275. Both items brand new. Full documentation. James R Fatz, 293 Indiana Av, Ft Wood MO 65473, (314) 368-5880.

WANTED: I have eight 1702A erasable read-only memories which I bought used on a printed circuit board. I would like to erase them, verify the erasure, program every bit, verify the programming, then erase the read-only memories, verifying the erasure. Finally, I need to have one read-only memory programmed for a keyboard encoder. Robert Heller, POB 51A Star Rt, Wendell MA 01379.

FOR SALE OR TRADE: For LSI-11, Heath H11, 11A owners. 4 K core (MMV11) used as small disk, keep loader, or BASIC in nonvolatile residence. $450, or trade for on board refreshed 16 K programmable memory module. C Chi, (617) 369-4000 ext 340 work; (617) 842-6326 home.

FOR TRADE: Have BYTE issues #1 and #4 in mint condition. Will trade for January, February, and May 1976 issues of BYTE in comparable condition. Will Hobbs, 1917 NE 8th #3, Portland OR 97212, (503) 284-5150.

WANTED: Ran out of space in my H11 system. I would like to trade my one each or two each H11-1, 4 K x 16 memory board plus reasonable cash for a single board 16 K x 16 memory board for H11. Must be in working condition. P Reyes, 86-115 Puhawai Rd, Waianae HI 96792, (808) 696-9329.

FOR SALE: Four Heath 4 K by 16 static-memory modules. Assembled and guaranteed working. Specify bank number and I will program before shipping. $200 each or $700 for all four. Harold Bula, 111 NW 8th Av #B4, Hallandale FL 33009.

FOR SALE: Heathkit ET-3400 microprocessor trainer in excellent condition with all manuals and programmed learning notebooks. Many additional chips and accessories. Nathan Coates, Rt 1 POB 44, Abilene TX 79601.

FOR SALE: 16 K, Level II TRS-80. Also, Tektronix type RM35A oscilloscope with type CA dual-trace plug-in unit and type D differential-input plug-in unit. TRS-80, $645. Oscilloscope with both plug-in units, $295. Richard J Aspey, 234 Beachwood Dr, Burbank CA 91506, (213) 842-7947.

ZILOG USERS: Zilog user seeks an exchange of ideas. Frank Light, 64 Errwood Rd, Manchester M19 2QH, ENGLAND.

FOR SALE: S&D Sales 4 K programmable memory, $50. Shugart SA-400 with power supply and cabinet, $290. Micromation PerSci double density, $2200. MITS serial input/output (I/O) board, $100. Vector Graphics read-only memory/programmable memory, $75. Ten 1702A read-only memories, $35. S&D cassette interface, $14. 3P + S I/O board, $130. Flexowriter with S-100 interface, punch, and reader, $375. Fred Manthey, POB 619, Mullan ID 83846, (208) 744-1143.

FOR SALE: S-100 boards: IA, Z80, Jade input/output (I/O), $100 each. SD 4 K programmable memory, $50. Digital cassette drive with control electronics, $50. PAIA 400 synthesizer, $300. Anthony Lassiter, 630 S Hermitage #402, Chicago IL 60612, (312) 942-4837.

WANTED: New or used dumb terminal and acoustic coupler, or a microcomputer with RS-232 interface and terminal capability. Lee Hayden, 5018 San Jose Blvd, Jacksonville FL 32207.

FOR SALE: Heath H8, H9, 24 K, dual cassettes, fully assembled and operational. Includes all assembly manuals, reference manuals, software (plus Extended BH BASIC with files), Space Wars game, *HUG library manual* and tape, and back issues of *REMark Magazine*. $1450/offer. J Scheip, 6487 Silver Ridge Cir, Alexandria VA 22310, (703) 971-9619.

FOR SALE: Micropolis 1043 Mod II, 315 K bytes formatted meta floppy disk. Complete with manual, newsletters, and S-100 bus-controller board. Moving up to larger system. First check for $950 takes all. Paul E Feick, 1105 Mala Dr, Layton UT 84041, (801) 376-9515 home, 524-4140 work.

WANTED: Newly formed computer club wants free games and/or other programs to run on a Level II TRS-80 system. Any consideration will be greatly appreciated. Bruce Caldwell, Draughon's Computer Club, Draughon's Junior College, 131 8th Av, Nashville TN 37203.

FOR SALE: Two Godbout Econoram II boards (static 8 K, 450 ns, S-100 bus) plus four spare 2102 memory integrated circuits. $90 each or nearest offer. I have switched to a 64 K Expendoram. Ron Subler, 25 First Parish Rd, Scituate MA 02066, (617) 545-6578.

FOR SALE: SwTPC CT-64, $275 and AC-30, $65. Professionally assembled, working, in as-new condition with documentation. R P Felton, 4803 Neblina Dr, Carlsbad CA 92008, (714) 729-5519.

FOR SALE: Digital Development Corp Model 12750 fixed head disk. 196 K bytes, 8.5 ms high-speed access. High reliability helium pressurized system with sixteen external track protect switches. Full documentation. Ideal for computer graphics database, or timeshare swapping storage. 19 inch side, 150 lbs, 115 VAC single phase; $500 plus shipping. J Zeglinski, 32 Aldgate Av, Toronto Ontario, CANADA M8Y 3L6.

FOR SALE: IMSAI 8080 or Cromemco Z2. Both contain full sockets and are equipped with North Star disk drive, Processor Tech 3P + S, and 8 to 32 K of memory. ADM3 terminals available and all my software for free. Best reasonable offer. J Roehrig, 7 Wildwood Dr, Dix Hills NY 11746, (516) 643-1931.

FOR SALE: Digital Group Z80 system. 26 K 21L02. Maxi-BASIC, Assembler, four input/output (I/O) ports, 64-character video board, power supply. Great system for Assembly or BASIC. $650. Preston Marshall, 8525 Monticello Av, Alexandria VA 22308, (703) 780-3768.

FOR SALE: Atari video computer system. Very good condition. Cartridges include Surround, Indy 500, Breakout, Outlaw, Air Sea Battle, Combat, Street Racer, Starship, Video Olympics, and Homerun. All handles for games come with system. System is worth $400, best offer takes it. Jody Wear, Rt 1 POB 83A, New Egypt NJ 08533, (609) 758-7193 after 3:30 PM.

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BOMB — BYTE's Ongoing Monitor Box

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September BOMB
Homebrewing: Soft Touch for Software

Congratulations to Mark Dahmke for his first place winning article "Introduction to Multiprogramming," September, page 20. An extremely close second place was taken by Steve Ciarcia's "Joystick Interfaces," page 10 with third place being awarded to William Powers, "The Nature of Robots," Part 4, page 96. ■



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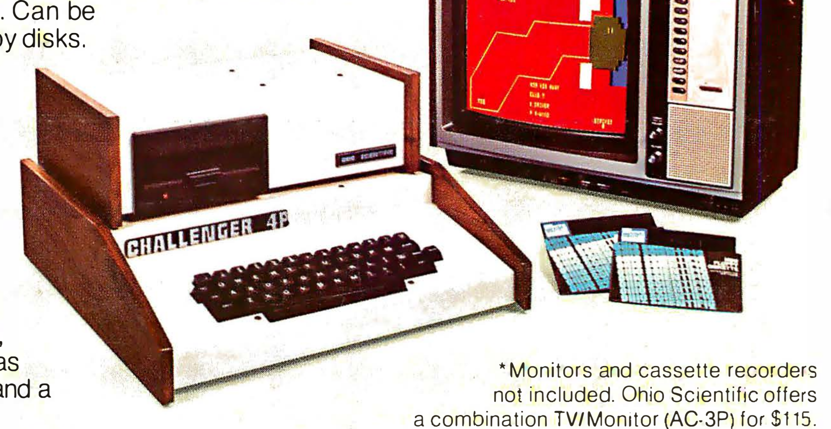
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